sciendo

Carpathian Journal of Electronic and Computer Engineering 12/1 (2019) 23-28

DOI: 10.2478/cjece-2019-0005

Modeling and Simulation of Single-Electron Transistor (SET) with Aluminum Island Using Neural Network

MOSTEFAI Abdelkrim
Applied Materials Laboratory, University of Sidi Bel Abbes,
22000- Sidi Bel Abbes, Algeria,
E-Mail: mostakrimo@yahoo.fr

***Abstract*— SET is important in the field of nanoelectronics since a decade. This paper presents electrical characteristic of Single-Electron Transistor (SET) with Aluminum Island using Neural Network. The I-V characteristic of the Single-Electron Transistor (SET) is predicted according to different parameters (V_G, T, V_D, C, and R). The simulation process is based on analytical transistor model and neural network transistor model. Single Electron Transistor (SET) is the simplest device in which the effect of Coulomb blockade can be observed.**

***Keywords*—Single-Electron Transistor (SET), Aluminum Island, nanoscale transistor, tunneling effects, coulomb blockade, MATLAB.**

I. INTRODUCTION

The Single Electron Transistor consists of an island connected through two tunneling junctions to a drain and a source electrode, and by means of a capacitor to a gate electrode, which is capable of offering low power consumption and high Operating speed [1,2]. The schematic diagram and of representation SET is shown in fig. 1. It is an essential element in device operation is based on one-by-one electron manipulation using the Coulomb blockade effect. Electrons are propagating from source to drain via an island. The energy of the electronic states on the island can be commanded through an electrostatic gate (fig. 2). Single-Electron Transistor (SET) is much appreciated in the field of nanoelectronics since a decade. This paper describes the electrical characterization for the Single-Electron Transistor (SET) with Aluminum Island (fig. 3) using neural network.

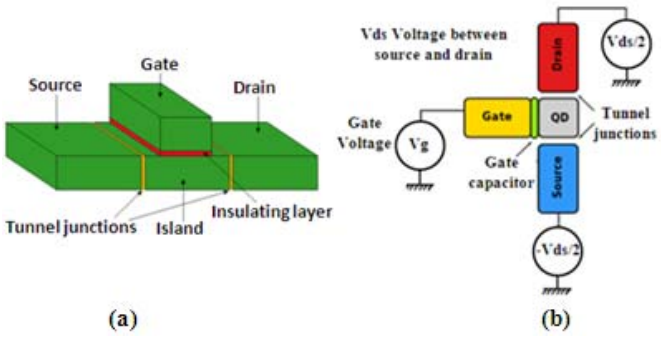

Fig. 1. (a) Representation of SET. (b) Schematic diagram of a Single-Electron Transistor.

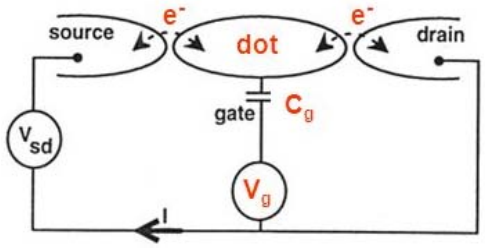

Fig. 2. Schematic figure of a nanoscale transistor.

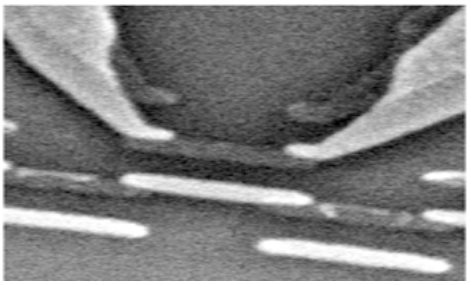

Fig. 3. Single-electron transistor Aluminum Island.

II. SINGLE ELECTRON TRANSISTOR

The principal three-terminal single-electron device is named Single Electron Transistor (SET) [3,4]. SET is practically the simplest device for present the effect of Coulomb blockade, which has been predicted by Kulik and Shekhter [5] as a physical phenomenon. A SET is primarily composed of three-terminal with gate, source, and drain, unlike quantum dots and resonant tunneling devices which may be two terminal devices without gates [6]. The circuit diagram of the SET is shown in fig. 4.

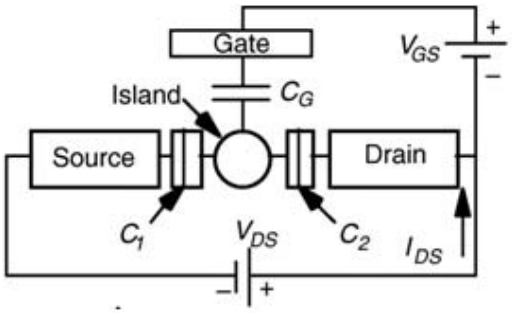

Fig. 4. Circuit diagram of the SET.

A. *Coulomb Blockade Effect*

The Single Electron Transistor (SET) differs from classic devices, in the sense that the electronic transport is controlled by quantum mechanics. The Coulomb blockade effect is the decrease in electrical conductance at small bias voltages of a small electronic device comprising at least one low-capacitance tunnel junction. Coulomb blockade is a mechanism studied in particular for the elaboration of Single-Electron Transistors. Because through of Coulomb blockade; we have the possibility to control the flow of carriers, electron by electron.

For Single Electron Transistor operation at finite temperature, the island should be low to maintain the Coulomb blockade condition; the charging energy is give as [7]:

$$E_C = e^2/2C_\Sigma \quad (1)$$

C_Σ is capacitance of this system ($C_\Sigma = C_1 + C_2 + C_G$).

Two important conditions are necessary for the tunneling operation:

One condition is that the charging energy E_C of single excess electron on quantum dot is much greater than the thermal energy is described by [8]:

$$E_C = e^2/2C_\Sigma > k_B T \quad (2)$$

Where k_B is Boltzmann's constant and T is temperature in Kelvin.

The other condition is that the electrons should be localized only on the island and all tunnel junctions should be opaque for electrons to confine them to the islands. This condition can be maintained if tunnel resistance R_T is larger than the quantum resistance R_Q.

$$R_T >> R_Q = h/e^2 = 25.813\ K\Omega \quad (3)$$

h is Planck's constant.

The tunneling rate Γ is given as [9]:

$$\Gamma = \frac{V}{eR_T} \quad (4)$$

B. *Basic Physics of SET (Single Electron Transistor) Operation*

The operation principle of a Single Electron Transistor (SET) is show in fig. 5. A Single Electron Transistor (SET) is a device whose operation based on single electron tunneling through a nanometric junction. The electrons tunnels are transmitted one-by-one through the channel (in contrast with classic MOSFET) due to its particular architecture that includes double tunneling junctions and one conductive island [10].

Figure 6 shows the Current-Voltage characteristics for the symmetric junction circuit for R_1=R_2 and C_1=C_2.

Figure 7 represents the Current-Voltage characteristics for a highly asymmetric junction circuit of Single Electron Transistor where R_1<<R_2 [12]. In this case the Current-Voltage characteristic represents the "Coulomb Staircase".

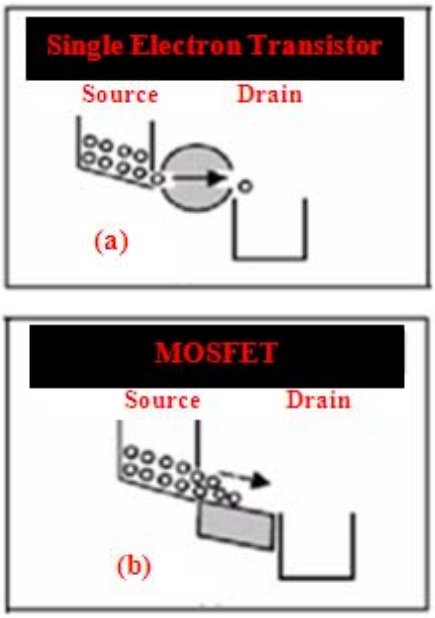

Fig. 5. Transfers of electrons is (a) one-by-one in SET (Single Electron Transistor), which is in contrast with (b) conventional MOSFET (Metal-Oxide-Semiconductor Field Effect Transistor) where many electrons simultaneously participate to the drain current [11].

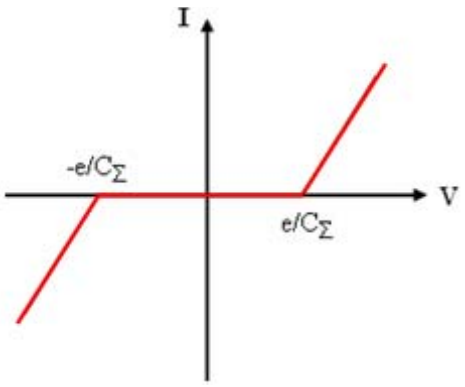

Fig. 6. I-V characteristics of SET, R_1=R_2 and C_1=C_2.

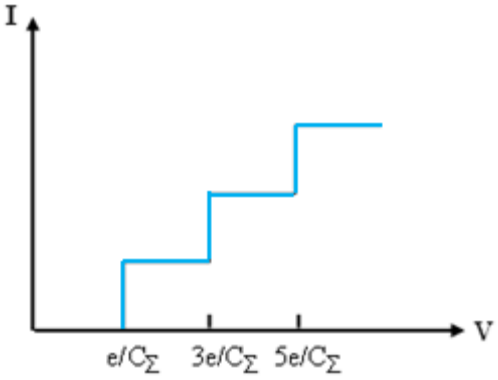

Fig. 7. I-V characteristics of the SET, R_1<<R_2.

III. MODELING AND SIMULATION OF SET

Various technique have been used for set modeling are analytical modeling [13], monte-carlo and macro method. A standard Single Electron Transistor circuit symbol is given in fig. 8. Single electron transistor has been envisaged as one of

the Component for future high-speed, high-density and low circuit applications.

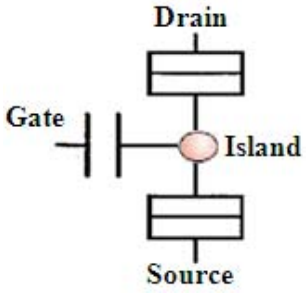

Fig. 8. The conventional circuit symbol for single electron transistor.

A. The Analytical Transistor Model

Different analytical models have been treated for Single Electron Transistor (SET) [14,15]. Uchida et al [15] propose an analytical model of Single Electron Transistor (SET), which has double tunneling junctions and additional capacitor connected to a conductive center island as present in fig. 9.

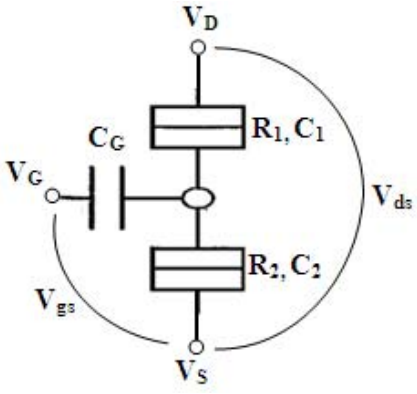

Fig. 9. Schematic of SET. The tunneling resistance of the source is assumed to be same as that of the drain.

The I-V characteristics of Single Electron Transistor (SET) having n or n+1 electrons in its island is given by [15]:

$$I_{D,n} = \frac{e}{2R_\Sigma C_\Sigma} \cdot \frac{\left(V_{gs}^2 - V_{ds}^2\right)\sinh(V_{ds}/T)}{V_{gs,n}\sinh\left(V_{gs}/T\right) - V_{ds,n}sinh(V_{ds}/T)} \quad (5)$$

Where

$$V_{gs,n} = \frac{2C_G V_{gs}}{e} - \frac{(C_G + C_2 - C_1)V_{ds}}{e} - 1 - 2n \quad (6)$$

$$V_{ds} = \frac{C_\Sigma V_{ds}}{e} \quad (7)$$

$$T = \frac{2k_B T C_\Sigma}{e^2} \quad (8)$$

$$R_\Sigma = R_1 + R_2 \quad (9)$$

$$C_\Sigma = C_1 + C_2 + C_G \quad (10)$$

Therefore, by incorporation $V_{gs,n}$= 0 in equation (6), the V_{gs} giving the peak of coulomb oscillations, we get:

$$V_{gs} = \frac{e}{2C_G} + \frac{ne}{C_G} + \frac{(C_G + C_2 - C_1)V_{ds}}{2C_G} \quad (11)$$

B. The Neural Network Transistor Model

The neural network (Multi-Layer Perceptron (MLP)) designed to connect the input vector (V_D, V_G, T, R and C) to output vector I_D. Each of these parameters is indexed by a neuron (fig. 10). The output activation function is the pure linear function (purelin), for hidden layers we choose the tangential sigmoid function (tansig). To enhance learning, we modified different parameters such as the number of neurons in the hidden layer.

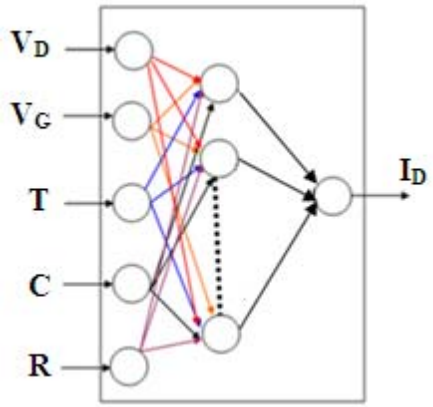

Fig. 10. The neuronal model of transistor SET (ANN-SET), Number of neuron of the hidden layer: 30.

TABLE 1 summarizes the characteristics of the network optimized of the SET.

TABLE I. CHARACTERISTICS OF THE NETWORK OPTIMIZED.

Propriety	Characteristic
Structure	30 -1 MLP
Function of activation	tansig-purelin
Learning rule	back propagation
EQM of test	10^{-23}
Iteration	1000 (not reached)

The program of learning is launched. One observes then at the same time the evolution of the error to each epoch (cycle of learning), then the function obtained by the network (fig.11).

The learning is excellent, with small parameters (limited number of neurons in the hidden layer), we obtain very good results (error about 10^{-23}).

Figures 12 and 13 represent the error surface and error contour of single input neuron (Sum of Squared Error (SSE) of prediction), for pure linear function transfer (purelin) and tangential sigmoid function transfer (tansig).

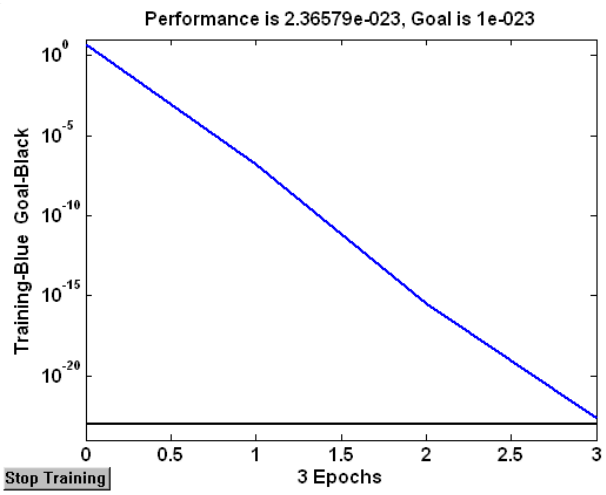

Fig. 11. Evolution of the average error of learning.

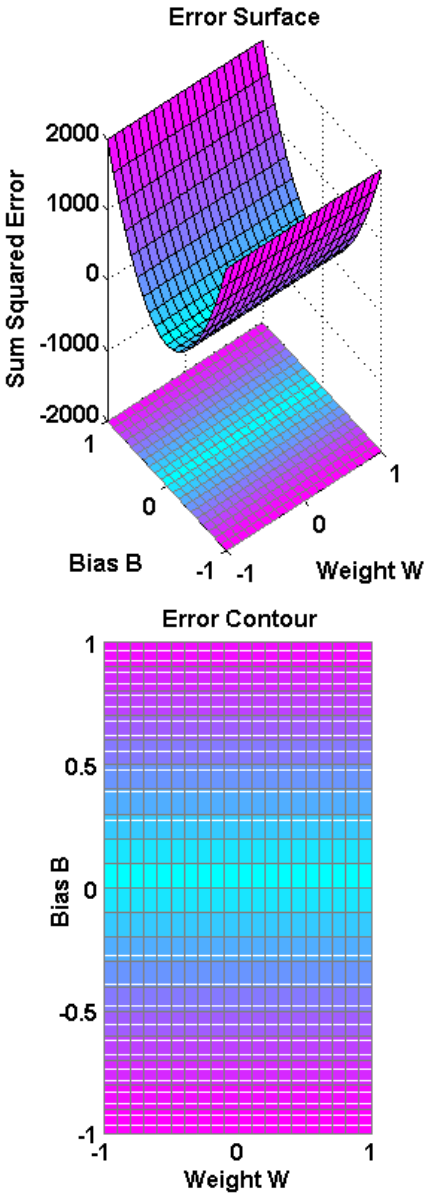

Fig. 12. Error surface and error contour of single input neuron (Sum of Squared Error (SSE) of prediction), pure linear function transfer (purelin).

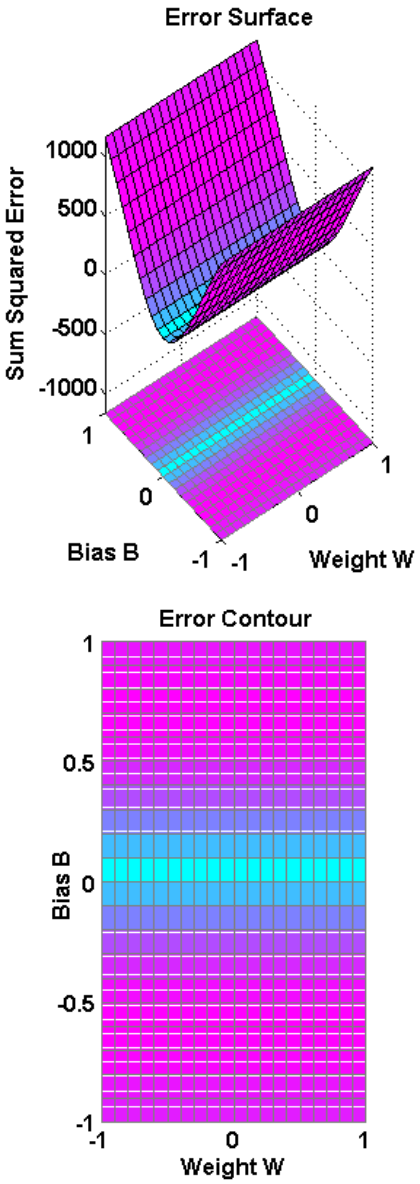

Fig. 13. Error surface and error contour of single input neuron (Sum of Squared Error (SSE) of prediction), tangential sigmoid function transfer (tansig).

IV. RESULTS AND DISCUSSION

SET model and ANN-SET model are implemented under Matlab m-file (program code), to plot different curves.

Figures 14 and 15 present a comparison between the results predicted by the neuronal model (ANN-SET) with those calculated by the analytical model for Aluminum Single Electron Transistors (SET). Figures 14, 15 and 16 represent the characteristics I-V of Aluminum Single Electron Transistors (SET) for different values gate voltage and temperature.

Figures 14 and 15 show the I-V characteristics for $R_1 = R_2 = 10^6\ \Omega$ and $C_1 = C_2 = 4.10^{-17}$ F. From the I-V characteristics of the SET, the current is zero that for -1 mV < V < 1 mV. This case is called Coulomb blockade that annuls the tunneling of single electron in case of low bias condition. If the externally applied junction voltage V is above the threshold voltage by charging energy, this effect of Coulomb blockade can be deleted and the current circulates.

Our objective here is to implement neural network programs in Matlab, using the backpropagation to identify different I-V characteristic of the SET. This model can be used to simulate the SET response to different parameters related to the manufacturing technology.

I_D-V_D characteristics calculated (simulated) by the neural network transistor model is compared with the analytical transistor model. It can be observed that excellent agreement between the neural and analytical data was obtained by both of the models.

The best advantage of artificial neural networks (ANNs) lies in their automatic learning capability, which allows solving problems without requiring writing complex rules. The results in this paper, in excellent agreement with precedent results Simulated with different methods (technique) applied to various Single Electron Transistors (SETs) models [16,17,18,19,20,21,22]. This last observation shows the applicability of the artificial neural network to the study of nanoscale CMOS circuits.

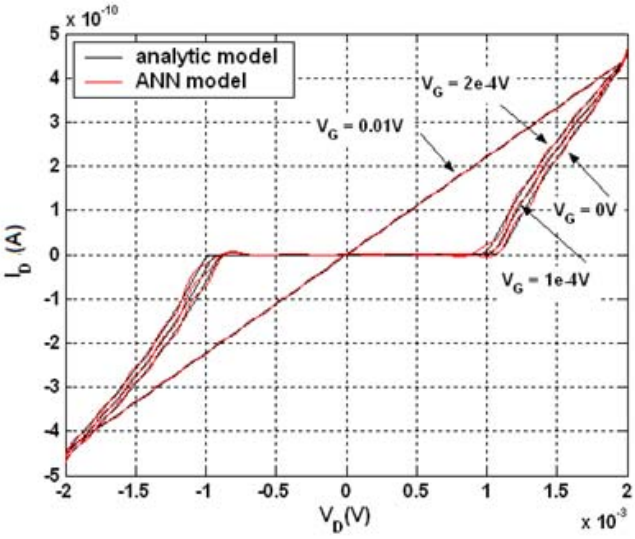

Fig. 14. I_D–V_D characteristics of the SET at T = 0.1 K.

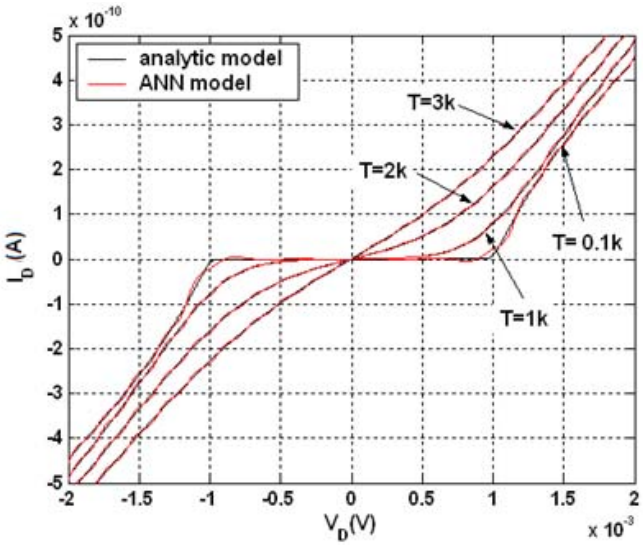

Fig. 15. I_D–V_D characteristics of the SET at Vg = 0 V.

Figure 16 shows the I-V characteristics for $R_1 << R_2$ (R_1 = 1 Ω, $R_2 = 10^6$ Ω) and $C_1 = C_2 = 2.10^{-16}$ F. The charge carrier's electrons penetrate through one junction and then evade to second junction due to the presence of high resistance. At present, electrons displaces from one junction to another very quickly. Thus this rapid displacement of excess electrons from one junction to another increase the total charge of the island, therefore, it will tend to increase the population of electrons. In this case the I-V characteristic represents the "Coulomb Staircase".

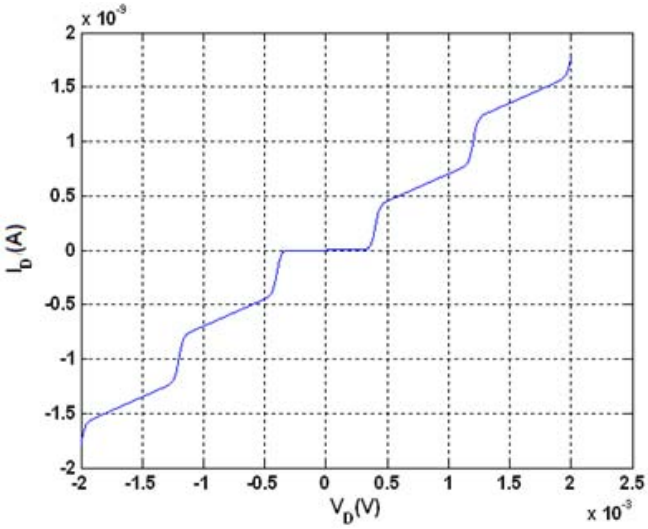

Fig. 16. I_D–V_D characteristics of the SET at $R_1 << R_2$ (R_1 = 1 Ω, $R_2 = 10^6$ Ω), T = 0.1 K, Vg = 0 V.

V. CONCLUSION

In this paper, we have presented I-V characteristics of the analytical and neural network model of Aluminum Single Electron Transistor implemented in MATLAB. Aluminum Single Electron Transistors (SET) are important concepts for analog circuit for the following reasons, Simple principle of operation, High operating speed, high sensitivity and Low energy consumption. Simulation and extracted parameter of Aluminum Single Electron Transistors (SET) are important to understand behavior of electron before designing and fabrication the devices.

REFERENCES

[1] L.J. Geerligs, V.F. Anderegg, P.A.M. Holweg, J.E. Mooij, H. Pothier, D. Esteve, C. Urbina, M.H. Devoret, "Frequency-locked turnstile device for single electrons," Phys. Rev. Lett, Vol. 64, pp. 2691-2694, 1990.

[2] H. Pothier, P. Lafarge, P.F. Orfila, C. Urbina, D. Esteve, M.H. Devoret, "Single electron pump fabricated with ultra-small normal tunnel junctions," Physica B, Vol. 169, N° 1-4, pp. 573-574, 1991.

[3] P. Hadley, G. Lientschnig, M-J. Lai, "Single-Electron Transistors," In Proceedings of the International Symposium. On Compound Semiconductors, pp. 1-8, 2002.

[4] K.K. Likharev, "Single-Electron Transistors: Electrostatic Analogs of the DC Squids," IEEE Trans. Magn, Vol. 23, pp. 1142-1145, 1987.

[5] I.O. Kulik, R.I. Shekhter, "Kinetic Phenomena and Charge Discreteness Effects in Granulated Media," Sov. Phys. JETP, Vol. 41, N° 2, pp. 308-316, 1975.

[6] D. Goldhaber-Gordon, M.S. Montemerlo, J.C. Love, G.J. Opiteck, J.C. Ellenbogen, "Overview of Nanoelectronic Devices," Proc. IEEE, Vol. 85, N° 4, pp. 521-540, 1997.

[7] Zahid A.K. Durrani, "Coulomb blockage, single electron transistor and circuit in silicon," physica E, Vol. 17, pp. 572-578, 2003.

[8] M. Khoury, A. Gunther, S. Milicic, J. Rack, S.M. Goodnick, D. Vasileska, T.J. Thornton, D.K. Ferry, "Single electron quantum dots in silicon MOS structures," Appl. Phys A, Vol. 71, N° 4, pp. 415-421, 2000.

[9] J. Hoekstra, R.H. Klunder, "Single Electron Transistor Circuit Simulation," Microelectronics Advanced Research Initiative (MEL-ARI) Answers, Technical Report, pp. 1-20, July 1998-July 1999.

[10] A.M. Ionescu, M.J. Declercq, S. Mahapatra, K. Banerjee, "Teaching Microelectronics in the Silicon ICs Showstopper Zone: A Course on Ultimate Devices and Circuits: Towards Quantum Electronics," In 4th European Workshop on microelectronics Educations (EWME), pp. 1-4, Baiona, Spain, May 23-24, 2002.

[11] K. Uchida, J. Koga, R. Ohba, A. Toriumi, "Programmable Single Electron Transistor Logic for Future Low-Power Intelligent LSI: Proposal and Room Temperature Operation," IEEE Trans. Electron Devices, Vol. 50, N° 7, pp. 1623-1630, 2003.

[12] V.P. Singh, A. Agrawal, S.B. Singh, "Analytical Discussion of Single Electron Transistor (SET)," International Journal Soft Computing and Engineering (IJSCE), Vol. 2, N° 3, pp. 502-507, 2012.

[13] Y-L. Wu, S-T. Lin, "Modeling of Single Electron Transistor – A Comparison between Macro-Model and Analytical Model," International Symposium on Nanoelectronic Circuits and Giga-Scale System (ISNCGS 2004), pp. 21-25, 2004.

[14] X. Wang, W. Porod, "Single Electron Transistor analytic I-V Model for SPICE Applications," Superlattices Microstruct, Vol. 28, N° 5/6, pp. 345-349, 2000.

[15] K. Uchida, K. Matsuzawa, J. Koda, R. Ohda, S-I. Takagi, A. Toriumi, "Analytical Single Electron Transistor (SET) Model for Design and Analysis of Realistic SET Circuits," Jpn. J. Appl. Phys, Vol. 39, pp. 2321-2324, 2000.

[16] B. Hafsi, A. Boubaker, I. Krout, A. Kalboussi, "Study and modeling neural memory based on single electron transistor using Simon simulator," 9th International Multi-Conference on Systems, Signals & Devices, pp. 1-6, Chemnitz, Germany, 2012.

[17] S. Mahapatra, K. Banerjee, F. Pegeon, A.M. Ionescu, "A CAD framework for co-design and analysis of CMOS-SET hybrid integrated circuits," International Conference on Computer Aided Design (ICCAD'03), pp. 497-502, San Jose, CA, USA, November 11-13, 2003.

[18] B. dos Santos Pês, J.G. Guimarães, E. Oroski, M.J. do Couto Bonfim, "A Spiking Neural Network implemented with Single-Electron Transistors and NoCs," Nano Commun. Networks, Vol. 17, pp. 21-29, 2018.

[19] Y.S. Yu, H.S. Lee, S.W. Hwang, "SPICE Macro-Modeling for the Compact Simulation of Single Electron Circuits," J. Korean Phys. Soc, Vol. 33, pp. S269-S272, 1998.

[20] C. Jia, H. Chaohong, S.D. Cotofana, J. Jianfei, "SPICE implementation of a compact single electron tunneling transistor model, " 4th IEEE Conference on Nanotechnology, pp. 392-395, 2004.

[21] N. Allec, R. Knobel, L. Shang, "Adaptive Simulation for Single-Electron Devices," Proceedings of the conference on Design, Automation and Test in Europe (DATE'08), Munich, Germany, pp. 1021-1026, March 10-14, 2008.

[22] P.K. Sinha, S. Sanjay, "Single Electron Transistor and its Simulation Methods," Int. J. Eng. Dev. Res, Vol. 2, N° 2, pp. 1907-1925, 2014.