sciendo
Power Electronics and Drives
Volume 9(44), 2024 DOI: 10.2478/pead-2024-0009



# A Study on Various Causes of Low Frequency Components in Common Mode Voltage of a Space Vector Pulse Width Modulated Three–Phase Quasi–Z–Source H–Bridge Inverter Fed from a Three–Phase Diode Bridge Rectifier

**Research paper**

Debalina Nanda*, Prasid Syam, Kaushik Mukherjee

*IIEST, Shibpur, Howrah, India*

**Received: 17 November 2023; Accepted: 30 January 2024**

**Abstract:** The presence of low frequency components in the common mode voltage can cause harmful electromagnetic interference. A critical study on various causes of low frequency components in the common mode voltage of a space vector pulse width modulated Quasi–Z–source three–phase H–bridge voltage source inverter fed from a three–phase diode bridge rectifier is presented in this paper. The Quasi–Z–source network is utilized in boosting the rectified dc voltage which increases the overall voltage gain. The study considers the effect of boosting on the low frequency components. The input three-phase diode bridge rectifier has its influence in modulating the instantaneous common mode voltage and contributes low frequency components. The unbalanced three-phase supply can contribute additionally ac supply frequency component in the common mode voltage. The major contribution of this paper is the analytical, simulated and experiment-based study on various causes of the low frequency common mode voltages due to the combined action of the input non-ideal three phase grid, the front-end diode bridge rectifier as well as the load-end Z-source H-bridge three-phase inverter feeding a three-phase inductive load, while operated through a space vector pulse width modulation strategy.

**Keywords:** *common mode voltage • Quasi–Z–source three phase H–bridge voltage source inverter • shoot–through duty ratio • simple boost control • low frequency spectrum*

## 1. Introduction

The conventional H-bridge voltage source inverter (VSI) has few limitations. The peak value of the ac line to line output voltages of a three-phase H-bridge VSI is at most the dc bus voltage for a “Space Vector Pulse Width Modulation” (SVPWM) scheme of switching pulse generation. This can be said as buck operation. Again, if this power circuit is, conversely, used for ac to dc rectification, then the dc voltage will be more than that applied ac input phase voltage. This can be called “a boost operation”. For a conventional three-phase H–bridge VSI, a dead time must be provided between state changes of the two switches in a leg to prevent short–circuit of the dc bus and destruction of the switches. A Z-source three–phase H–bridge VSI employs an impedance network (Z–network) consisting of an inductor (L), a capacitor(C) and a diode along with the conventional converter (Peng, 2003). So, there is no need to provide additional dead time between the transitions of states of the switches in a leg of the converters. This additional network with shoot-through states can be used to boost and buck operation whenever

* *Email: debalinananda91@gmail.com*

needed (Peng, 2003; Peng et al., 2003; Peng et al., 2005a, Roomi, 2019). This Z–network also restricts the amount of shoot-through current within an allowable limit. So, there is no need to provide additional dead time between the transitions of states of the switches in a leg of the converters. There exist two types of Z–network: 1.) Normal Z–network and 2.) Quasi Z- network. The Quasi Z–network is advantageous because it maintains continuous dc input current (Anderson et al., 2008; Gajanayake et al., 2010; Nguyen et al., 2011; Vinnikov et al., 2011; Sabat et al., 2022). Here voltage fed three–phase H–bridge Quasi Z–source inverter (Q–ZSI) is considered for study. For switching pulse generation, the SVPWM scheme is implemented for better dc bus utilization (Cacciato et al., 2009; Loh et al., 2005; Nanda et al., 2019). The work has considered simple–boost control (SBC) where shoot-through pulse duration remains constant for a particular boosting factor (Peng et al., 2005b).

The dc source for the study in this paper is a three–phase bridge rectifier supplied from a three–phase ac supply (grid) as shown in the Fig. 1. The common mode voltage (CMV) is defined as the voltage of the Quasi Z source inverter's (Q–ZSI) load star point with respect to the grid side neutral point as shown in Fig. 1 (Ün et al., 2009). The CMV is expressed in terms of the output phase voltages with respect to the ac grid neutral as in (1).

$$\begin{aligned} v_{cmv} &= v_{ng} \\ &= (v_{Ag} + v_{Bg} + v_{Cg})/3 \end{aligned} \tag{1}$$

The appearance of common mode voltage (CMV) at the output voltages of the inverter with respect to the ac grid neutral is inevitable due to various reasons (Akagi et al., 2004; Cacciato et al., 1999; Chatterjee et al., 2023b, Chen et al., 2019; Hava et al., 2011; Hou et al., 2013; Ün et al., 2009; Lai et al., 2004).The frequency components of the CMV can be broadly classified as low frequency and high frequency components. The components having frequencies close to and above the switching frequency of the SVPWM pulses are the high frequency components and the components which are close to the desired output frequency, are the low frequency components. If the load neutral is connected to the earth for safety reason, then a common mode current flows to the earth (Mirzaeva et al., 2020; Zhu et al., 2012). The low-frequency common mode currents flowing through the wires create low frequency magnetic field in the near surrounding. This low frequency magnetic fields affect the sensitive equipment. These low-frequency components are harmful in the naval ship and submarines as the power systems for navy ships and submarines cannot be grounded to the earth. The power line filter capacitors provide a path for conducting current through the hull ground structure. The navy utilises very sensitive low frequency radio and sonar receivers. At low frequencies, currents flowing through the installation structure and across surfaces of electronic enclosures penetrate to the inside of the enclosure. The magnetic fields created by these low frequency currents can couple into critical circuits and degrade performance. The metallic body cannot shield these low frequency currents (MIL-STD-461F, 2007). These low frequency components in the CMV cannot be easily filtered out from the output of the inverter (Chen et al., 2016; Chen et al., 2019; Oliveira et al., 2017;Tan et al., 2019; Tian et al., 2016; Huang et al., 2014). In the analysis considering SVPWM, the CMV is approximately defined as the voltage of the load star point with respect to the mid-point voltage of the rectified dc voltage (Hava et al., 2011; Hou et al., 2013; Ün et al., 2009). But this restricts the analysis which cannot explain the appearance of third harmonic of the grid frequency component in the CMV with respect to the ac grid neutral (Akagi et al., 2004; Akagi et al., 2006). Additionally, it is observed under this study that a small unbalance in the three–phase grid gives rise to supply grid frequency component in the common mode voltage. It is observed that, for a Q–ZSI, the similar low frequency components of CMV are present. But the magnitudes of those components can differ due to the presence of shoot-through

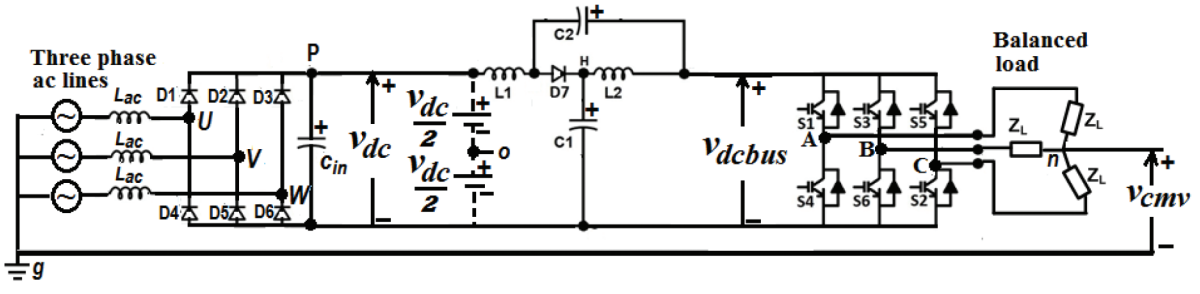


**Fig. 1.** Power circuit schematic of three–phase bridge rectifier fed Q–ZSI.

time duration. All these aspects are considered. The pulse generation scheme for the Q–ZSI to accommodate the shoot– through in SVPWM is implemented in a Field Programming Gate Arrays (FPGA) based development board. Both the simulation and experimental results are included in the study.

## 2. Switching pulse generation

The Q–ZSI has a network consisting of inductor (L), capacitor (C) and a diode which helps in boosting the dc-link voltage and assures continuous dc input current (Anderson et al., 2008). The idealized electrical circuit schematic for the analysis of Q–ZSI is shown in Fig. 2. The input dc source ($V_{in}$) for the experiment purpose is provided by employing a three–phase bridge rectifier. The boosted dc voltage ($v_{dcB}$) appears as the dc bus voltage for the VSI. The conventional SVPWM is considered here for the H-bridge VSI. It utilizes six active vectors and two zero vectors to generate the rotating space vector. The shoot–through time period for the Q–ZSI is placed within the zero-state time interval so that it cannot influence the active state (Loh et al., 2005; Nanda et al., 2019). The duration of shoot–through time period helps in deciding the boost–factor. To work with a fixed boost–factor, the SBC is considered in this study i.e. only a fixed portion of the zero-state time interval is converted to shoot-through state (Peng et al., 2005). There are two modes of operation in such a converter: a) shoot–through state and b) non–shoot–through state. The equivalent electrical circuit for the two modes are shown in Fig. 3.

The typical waveforms of different currents and voltages with respect to Fig. 3 are shown in Fig. 4. The current through the inductor L1 ($i_{L1}$) also represents the current drawn from the input dc source ($V_{in}$). During shoot-through duration, the voltage at dc bus of the VSI falls to zero. The inductor current ($i_{L1}$) increases to gain energy during the

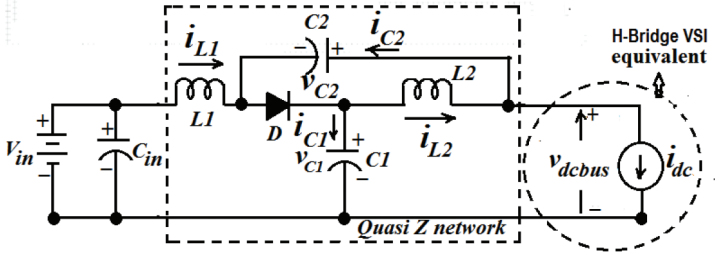


**Fig. 2.** Equivalent electrical circuit for a Q–ZSI.

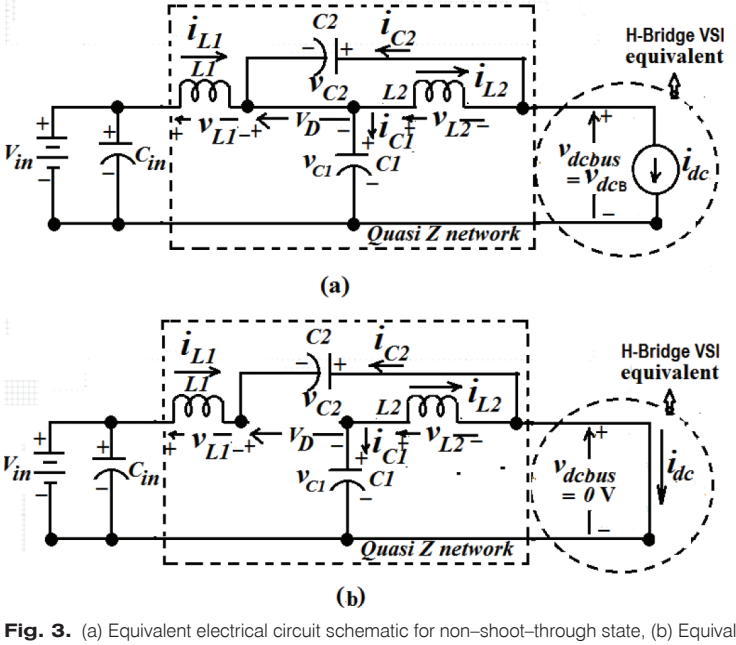


**Fig. 3.** (a) Equivalent electrical circuit schematic for non–shoot–through state, (b) Equivalent electrical circuit schematic for shoot–through state.

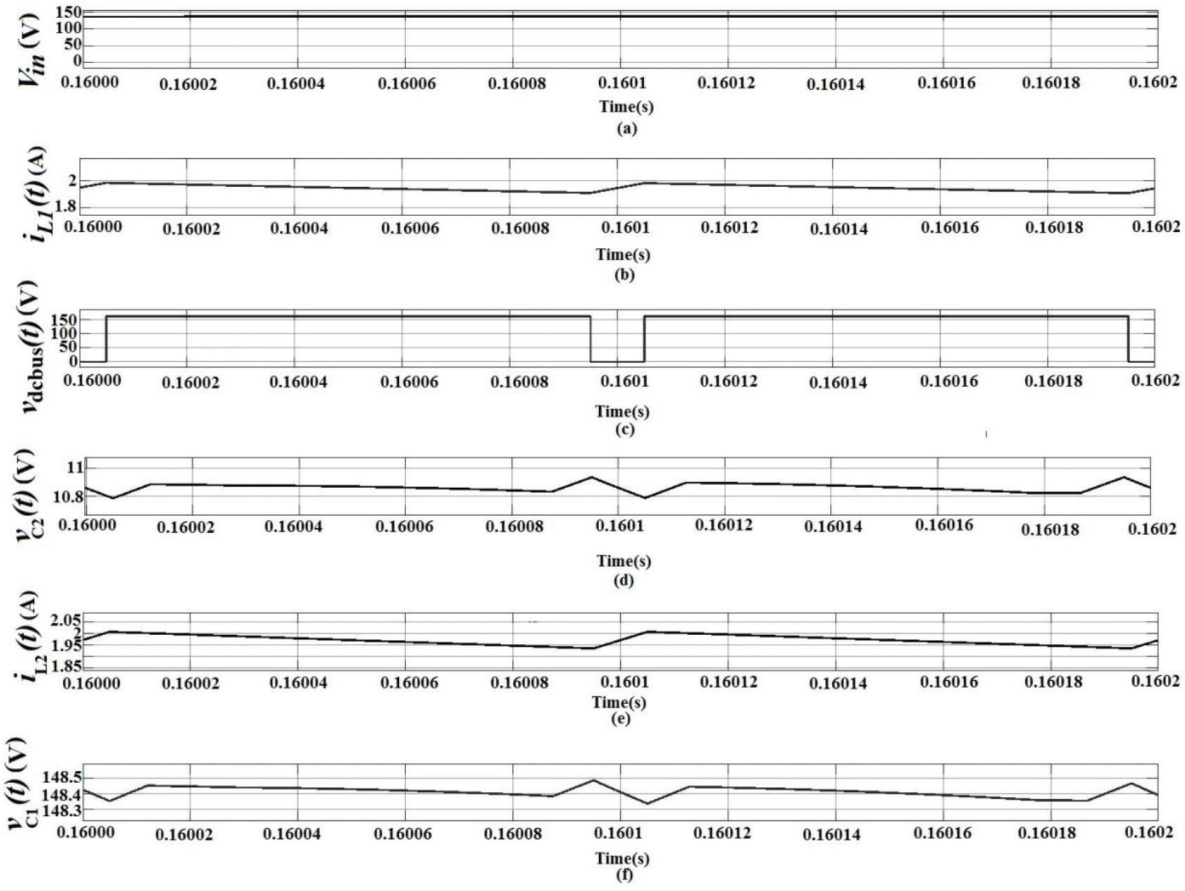


**Fig. 4.** Different waveforms obtained through simulation for the electrical circuit shown in Fig. 3: (a) Input dc voltage ($V_{in}$), (b) Input current ($i_{L1}$) through the inductor "L1", (c) dc bus voltage at the inverter end ($v_{dcbus}$), (d) voltage across capacitor "C2" ($v_{C2}$), (e) current ($i_{L2}$) through the inductor "L2", (f) voltage across capacitor "C1" ($v_{C1}$), (g) dc bus current at the inverter end.

shout-through duration. The capacitor C2 is then discharging. The current flowing through the inductor L2 ($i_{L2}$) also increases during shoot-through duration while discharging the capacitor C1. During non-shoot-through duration, the inductor currents decreases and the capacitor voltages begins to rise again. The voltages across the two capacitors ($v_{C1}$ and $v_{C2}$ ) add to provide boosted dc bus voltage ($v_{dcbus}$). The voltages across the capacitors rises faster during the dwelling time of the "zero" states as no power is transferred to the load side.

Considering a fixed shoot–through duty ratio ($d_{sh}$), the boosted dc ($v_{dcB}$) voltage during the non-shoot through state can be expressed as:

$$v_{dcB} = \frac{1}{1-2d_{sh}} \times V_i \tag{2}$$

The boost-factor "B" is defined as:

$$B = \frac{1}{1-2d_{sh}} \tag{3}$$

The output ac peak line-to-line voltage for SVPWM can be expressed as:

$$V_{ac(peak)} = m \times V_{dcB} \tag{4}$$

Where, "*m*" is the modulation index. Therefore,

$$V_{ac(peak)} = m \times \frac{1}{1-2d_{sh}} \times V_{in} \tag{5}$$

In simple boost control [10], the relation between maximum shoot–through duty ratio ($d_{shmax}$) and modulation index ($m$) is:

$$d_{sh\max} = 1 - m \tag{6}$$

The space vector pulse width modulation for the H–bridge VSI of the Q–ZSI utilizes six active vectors and two zero vectors to generate rotating space vector (Liu et al., 2014). The desired output line–to–line voltages are defined as in (7)–(9),

$$v_{AB} = V_m \sin(2\pi f_o t) \tag{7}$$

$$v_{BC} = V_m \sin\left(2\pi f_o t - \frac{2\pi}{3}\right) \tag{8}$$

$$v_{CA} = V_m \sin\left(2\pi f_o t + \frac{2\pi}{3}\right) \tag{9}$$

Where, ($f_o$) is the output voltage frequency in Hz, ($t$) denotes time in seconds and ($V_m$) is the peak value of the line–to–line voltage in volts.

The rotating output voltage space vector is derived in (10).

$$\begin{aligned}\vec{v}_o &= \frac{2}{3}\left(v_{AB} + v_{BC} \times e^{j\frac{2\pi}{3}} + v_{CA} \times e^{j\frac{4\pi}{3}}\right) \\ &= V_m e^{j\left(2\pi f_o t - \frac{\pi}{2}\right)}\end{aligned} \tag{10}$$

The boosted dc bus voltage creates six stationary active vectors and two zero vectors with the different allowable switching combinations. Additionally, for Q–ZSI, the shoot-through states are created by switching "on" at least two switches in the same leg. The conventional allowable switching states are shown in Table 1 excluding shoot-through states. The states of switches are indicated by the numbers "1" and "0". Here, "1" stands for "devices in Switched-On" condition and "0" stands for "devices in Switched–off" condition. The states of the switches are given in a matrix format. The shoot–through states do not give rise to a stationary space vector as the dc bus becomes short-circuited.

The switching state stationary space vectors for active states and rotating desired voltage vector are shown in Fig. 5.

At any instant of time, the rotating vector ($\vec{V}_o$) can be constructed by taking components from the neighbouring stationary active space vectors as illustrated in the Fig. 5. There are six different sectors separated by six active stationary vectors as shown in Fig. 5. Considering the positive rotation of the output voltage space vector in anti-clockwise direction, two active stationary vectors can be identified in each of the sectors: one just behind the rotating vector ($\vec{V}_b$) and the other just ahead of the rotating vector ($\vec{V}_f$) as shown in Fig. 5 for sector–1. The duty ratio of the vector is defined as the fraction determining the ratio of the magnitude of the component to the magnitude of the stationary space vector. Therefore, two active duty ratios are determined for the two participating active vectors. The duty ratio for the zero vectors is determined by subtracting the summation of the two active vectors' duty ratio from the value one. After computation of the duty ratio and knowing the participating stationary active vectors and the zero vectors, the dwelling time of different stationary vectors are generated. The dwelling time of the shoot–through states are kept within the dwelling time of the zero vectors. A typical distribution of dwelling times is shown in Fig. 6.

**Table 1.** Different switching state stationary space vectors.

| Switching states $\begin{bmatrix} S1 & S3 & S5 \\ S4 & S6 & S2 \end{bmatrix}$ | Magnitude, volt | Angle, radian | Assigned name |
|---|---|---|---|
| $\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 1 \end{bmatrix}$ | $\frac{2}{\sqrt{3}}V_{dcB}$ | $\frac{\pi}{6}$ | $\vec{V}_1$ |
| $\begin{bmatrix} 1 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$ | $\frac{2}{\sqrt{3}}V_{dcB}$ | $\frac{\pi}{2}$ | $\vec{V}_2$ |
| $\begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 1 \end{bmatrix}$ | $\frac{2}{\sqrt{3}}V_{dcB}$ | $\frac{5\pi}{6}$ | $\vec{V}_3$ |
| $\begin{bmatrix} 0 & 1 & 1 \\ 1 & 0 & 0 \end{bmatrix}$ | $\frac{2}{\sqrt{3}}V_{dcB}$ | $-\frac{5\pi}{6}$ | $\vec{V}_4$ |
| $\begin{bmatrix} 0 & 0 & 1 \\ 1 & 1 & 0 \end{bmatrix}$ | $\frac{2}{\sqrt{3}}V_{dcB}$ | $-\frac{\pi}{2}$ | $\vec{V}_5$ |
| $\begin{bmatrix} 1 & 0 & 1 \\ 0 & 1 & 0 \end{bmatrix}$ | $\frac{2}{\sqrt{3}}V_{dcB}$ | $-\frac{\pi}{6}$ | $\vec{V}_6$ |
| $\begin{bmatrix} 1 & 1 & 1 \\ 0 & 0 & 0 \end{bmatrix}$ | 0 | - | $\vec{V}_7$ |
| $\begin{bmatrix} 0 & 0 & 0 \\ 1 & 1 & 1 \end{bmatrix}$ | 0 | - | $\vec{V}_0$ |

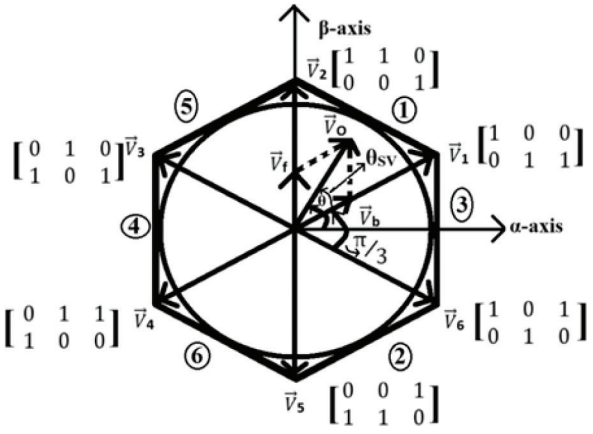


**Fig. 5.** Switching state active stationary space vectors and the output line–to–line voltage rotating space vector.

"$d_b$" is the duty ratio for the stationary space vector ($\vec{V}_b$) and "$d_f$" is the duty ratio for the stationary space vector ($\vec{V}_f$). "$d_o$" is duty ratio for the zero vectors. The "$T_b$" is the dwelling time for the stationary space vector ($\vec{V}_b$) and "$T_f$" is the dwelling time for the stationary space vector ($\vec{V}_f$). "$T_o$" is the dwelling time for the zero vectors. "$T_{sh}$" is the dwelling time of the shoot-through state. The dwelling times are distributed symmetrically over the switching time period "$T_s$". For SBC, the dwelling time of the shoot-through state does not vary and it resides with the dwelling time of the zero vectors ((Liu et al., 2014). The selection of this dwelling time is very important in SBC to achieve a required overall gain by adjusting the boost factor "$B$" and the modulation index "$m$". The minimum dwelling time of the zero vectors is equal to {(1-$m$) × $T_s$}.Therefore, the dwelling time of the shoot-through state should not exceed {(1-$m$) × $T_s$}.

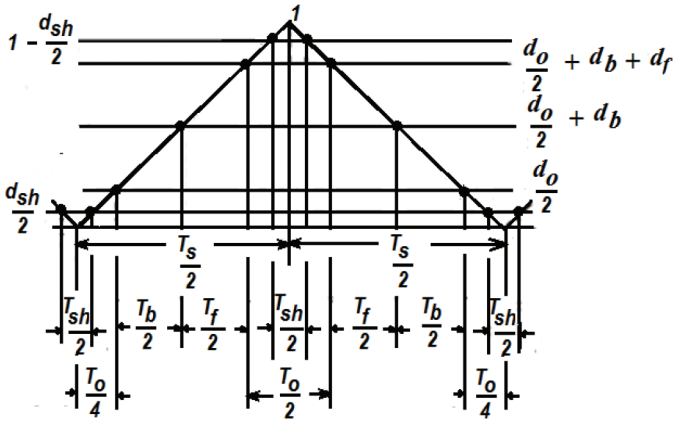


**Fig. 6.** Typical dwelling times for different switching state stationary vectors and shoot-through state.

## 3. Cause of low frequency components in the CMV

The CMV, as defined in (1), can be extended further to relate the dc bus voltage with respect to grid neutral in the expression in (11).

$$\begin{aligned} v_{cmv} &= v_{ng} \\ &= (v_{Ag} + v_{Bg} + v_{Cg})/3 \\ &= (v_{Ao} + v_{og} + v_{Bo} + v_{og} + v_{Co} + v_{og})/3 \\ &= (v_{Ao} + v_{oP} + v_{Pg} + v_{Bo} + v_{oP} + v_{Pg} + v_{Co} + v_{oP} + v_{Pg})/3 \\ &= (v_{Ao} - \frac{v_{dc}}{2} + v_{Pg} + v_{Bo} - \frac{v_{dc}}{2} + v_{Pg} + v_{Co} - \frac{v_{dc}}{2} + v_{Pg})/3 \\ &= (v_{Ao} + v_{Bo} + v_{Co})/3 - \frac{v_{dc}}{2} + v_{Pg}) \\ &= v_{no} - \frac{v_{dc}}{2} + v_{Pg} \end{aligned} \tag{11}$$

Where,

$$v_{no} = (v_{Ao} + v_{Bo} + v_{Co})/3 \tag{12}$$

The term $v_{no}$ represents the load neutral point voltage with respect to the virtual mid–point terminal potential of the rectified dc output. The virtual mid-point terminal “o” is not physically available terminal in the Fig. 1. But for the analytical purpose the terminal is conceptualised. In case of pure dc source made up of electrical battery, this terminal is available. Then the potentials of all other nodes are referred with respect to this terminal. The variable $v_{no}$ has the low frequency component at the third harmonic of the output desired frequency in the CMV (Akagi et al., 2004; Ün et al., 2009; Fan et al., 2023; Hava et al., 2011).The term $v_{Pg}$ represents the potential of the positive bus terminal “P” of the rectified dc output with respect of the potential at the ac grid neutral terminal ”g” in the Fig. 1. The ripple in this potential causes third harmonic of the grid frequency component in the CMV. The contribution of other variables in (11) is to produce the low frequency component at the third harmonic of the grid frequency for a three–phase balanced supply (Akagi et al., 2004; Smolenski et al., 2010; Zhu et al., 2012). The variable $\left(\frac{v_{dc}}{2}\right)$ is not a constant term. It contains ripple at third harmonic of grid frequency. For small unbalance in the ac mains supply/ grid voltage, those other variables produce grid frequency component in the CMV.

The time–variation of the CMV and the time–variation of the different components constituting the CMV in (12) are plotted in Fig. 7. Those are obtained through simulation. In the simulation study, the input ac supply voltage

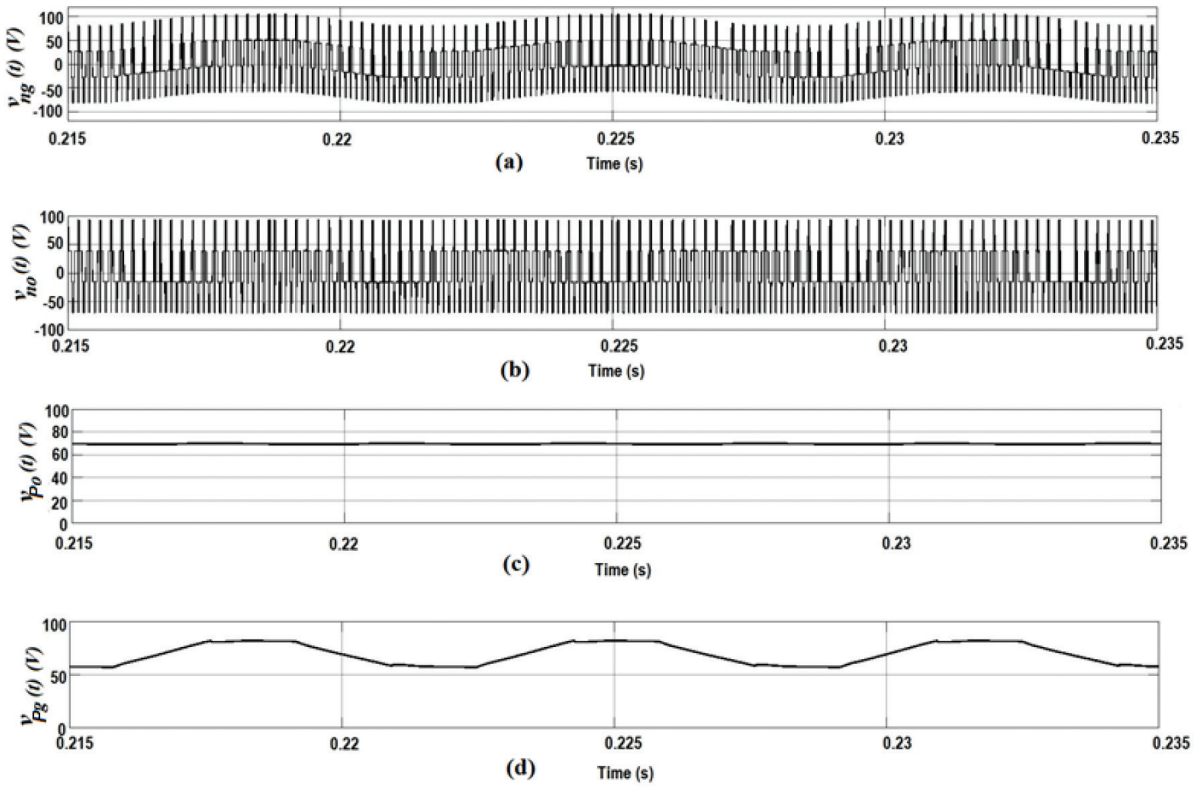


**Fig. 7.** (a) The waveform of the common mode voltage with respect to the three phase ac grid neutral terminal ($v_{ng}$), (b) The waveform of the common mode voltage with respect to virtual mid-point potential of the rectified voltage ($v_{no}$), (c) The waveform of the voltage of the positive terminal of the rectified dc with respect to the virtual mid-point potential of the rectified voltage ($v_{Po}$), (d) The waveform of the voltage of the positive terminal of the rectified dc with respect to the three phase ac grid neutral terminal ($v_{Pg}$). Grid voltage: three-phase 100V, 50 Hz, line–to–line. Shoot-through duty ratio: 0.1, modulation index: 0.8 and desired output voltage frequency: 80 Hz.

**Table 2.** Electrical circuit parameters considered for simulation study.

| Circuit parameters | Value |
|---|---|
| Capacitance of the dc filter capacitor ($C_{in}$) | 2000 microF |
| Inductance of Z–network inductor ($L_1$) | 20 mH |
| Inductance of Z–network inductor ($L_2$) | 20 mH |
| Capacitance of Z–network capacitor ($C_1$) | 140 microF |
| Capacitance of Z–network capacitor ($C_2$) | 140 microF |
| Load Inductance per phase | 20 mH |
| Load Resistance per phase | 29 ohms |

is considered three–phase 100V, 50 Hz, line–to–line. The three–phase load is passive inductive load. The circuit parameters considered for simulation study is given in Table 2. The parameter values are rounded to the nearest integer. The output desired frequency is considered 80 Hz. The switching frequency in the SVPWM is considered 5 kHz. The instantaneous CMV ($v_{ng}$) clearly shows the impression of the low frequency component at the third harmonic of the grid frequency in the envelope of the waveform as shown in the Fig. 7(a). The envelope of the voltage waveform $v_{no}$, in Fig. 7(b) does not show the presence of low frequency component at the third harmonic of the grid frequency. Therefore, presence of third harmonic component cannot be detected if the CMV is defined as the potential of load star point with respect to the virtual mid-point potential of the rectified dc voltage. The instantaneous waveform of $v_{Po}$ shows a small presence of variation of a sixth harmonic of the three phase ac grid frequency, as apparent in Fig. 7(c).The instantaneous waveform of P–terminal of the rectifier ($v_{Pg}$) shows the periodic variation of the waveform with a frequency of thrice of the grid frequency in the Fig. 7(d). This is the cause

**Table 3.** Common mode voltage with respect to the virtual mid-point potential of the rectified dc voltage.

| Switching state | Common mode voltage |
|---|---|
| $\begin{bmatrix}1&0&0\\0&1&1\end{bmatrix}(\bar{V}_1)$ | $\frac{1}{3}B\times v_{dc}-\frac{1}{2}v_{dc}$ |
| $\begin{bmatrix}1&1&0\\0&0&1\end{bmatrix}(\bar{V}_2)$ | $\frac{2}{3}B\times v_{dc}-\frac{1}{2}v_{dc}$ |
| $\begin{bmatrix}0&1&0\\1&0&1\end{bmatrix}(\bar{V}_3)$ | $\frac{1}{3}B\times v_{dc}-\frac{1}{2}v_{dc}$ |
| $\begin{bmatrix}0&1&1\\1&0&0\end{bmatrix}(\bar{V}_4)$ | $\frac{2}{3}B\times v_{dc}-\frac{1}{2}v_{dc}$ |
| $\begin{bmatrix}0&0&1\\1&1&0\end{bmatrix}(\bar{V}_5)$ | $\frac{1}{3}B\times v_{dc}-\frac{1}{2}v_{dc}$ |
| $\begin{bmatrix}1&0&1\\0&1&0\end{bmatrix}(\bar{V}_6)$ | $\frac{2}{3}B\times v_{dc}-\frac{1}{2}v_{dc}$ |
| $\begin{bmatrix}1&1&1\\0&0&0\end{bmatrix}(\bar{V}_7)$ | $B\times v_{dc}-\frac{1}{2}v_{dc}$ |
| $\begin{bmatrix}0&0&0\\1&1&1\end{bmatrix}(\bar{V}_0)$ | $-\frac{1}{2}v_{dc}$ |
| Shoot–through | $-\frac{1}{2}v_{dc}$ |

of the low frequency component at the third harmonic of the three phase ac grid frequency in the CMV at the output of the Q-ZSI under study in this paper.

The peak value of the low frequency component at the third harmonic of the grid frequency in the CMV is nearly equal to the magnitude of the third harmonic component present in the voltage at the P-terminal of the output of the bridge rectifier with respect to the three phase AC grid neutral (Akagi et al., 2004). This peak value at the third harmonic of the grid frequency in the CMV depends on the filter capacitance and the dc load current drawn from the bridge rectifier. For an unfiltered rectifier output, considering negligible voltage drop across the diodes and zero commutation intervals in the diode bridge rectifier, this peak value of the low frequency component at the third harmonic of the grid frequency in the CMV is nearly 20.61% of the peak value of the ac grid phase voltage.

The cause of the low frequency component at the third harmonic of the output desired frequency in the CMV in a traditional two-level H-bridge inverter with constant dc bus voltage is due to the fact that sum of the instantaneous output voltages in different phases with respect to dc mid-point potential is not zero (Tian et al., 2016). During active states, for example in the duration of stationary switching state vector ($\bar{V}_2$), the output terminal "A" is connected to positive dc bus having the voltage ($V_{dcB}$) with respect to the negative terminal of the dc bus. The output terminal "B" is connected to positive dc bus having the voltage ($V_{dcB}$) and the output terminal "C" is connected to negative dc bus having the voltage zero volt. With respect to the potential at the conceptual terminal "o", the voltage ($v_{Ao}$) is equal to $\left(V_{dcB}-\frac{V_{dc}}{2}\right)$, the voltage ($v_{Bo}$) is equal to $\left(V_{dcB}-\frac{V_{dc}}{2}\right)$ and the voltage ($v_{Co}$) is equal to $\left(-\frac{V_{dc}}{2}\right)$. As a result, the instantaneous summation of these three voltages at the output terminals is equal to $\left(2V_{dcB}-3\times\frac{V_{dc}}{2}\right)$ which is not zero. This generates the voltage component ($v_{no}$) in the expression (11) and (12). The algebraic addition of other two voltage components $\left(-\frac{v_{dc}}{2}+v_{Pg}\right)$, in the expression (11), give rise to third harmonic component at grid frequency. A similar observation is applicable for the duration of any one of the active states. For zero states, the three phase output terminals are connected simultaneously to either positive dc bus or negative dc bus voltage. In shoot-through states, all the output phase terminals are connected to negative dc bus voltage. For a constant dc bus voltage, the CMV with respect to the dc mid-point voltage shows third harmonic of the output desired frequency

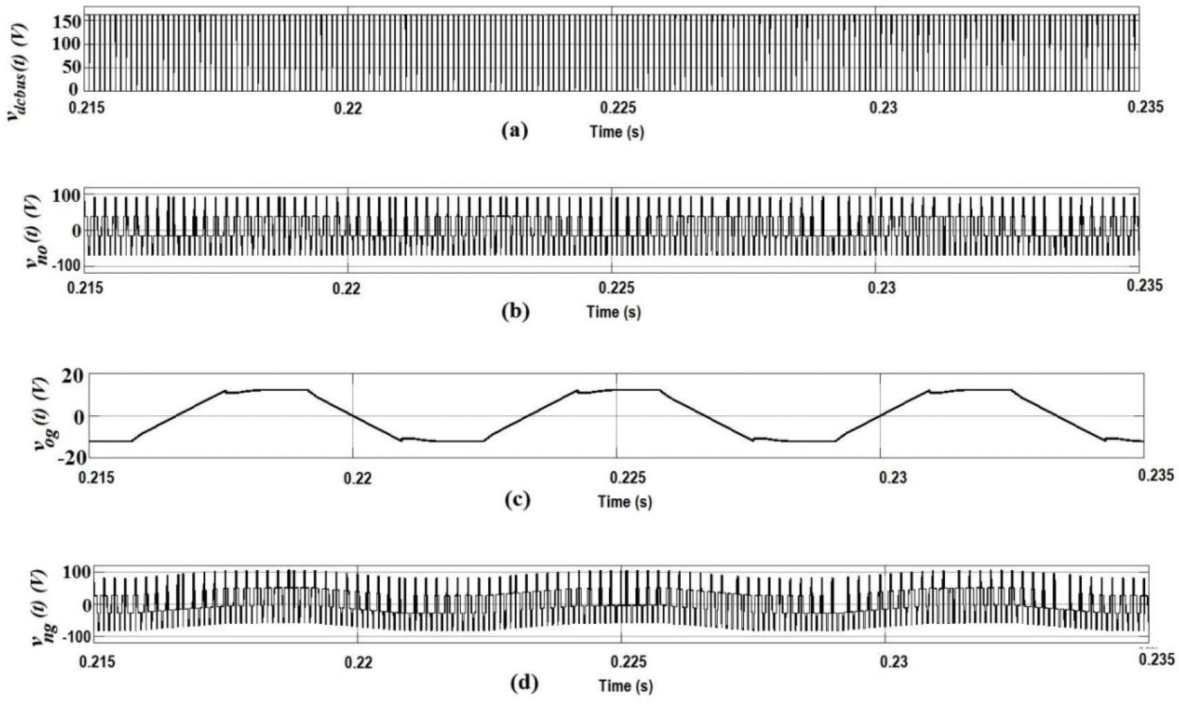


**Fig. 8.** (a) The waveform of the inverter dc bus voltage ($v_{dcbus}$), (b) The waveform of the voltage of load star point with respect to virtual mid-point potential of the rectified voltage ($v_{no}$), (c) The waveform of the virtual mid-point potential of the rectified voltage with respect to the three phase ac grid neutral ($v_{og}$), (d) The waveform of the CMV ($v_{ng}$). Grid voltage: Three-phase line–to–line 100V, 50 Hz, Shoot-through duty ratio: 0.1, modulation index: 0.8 and desired output voltage frequency: 80 Hz.

(Tian et al., 2016). For a Q–ZSI, the magnitude of this third harmonic component depends on the boost-factor "B" (Jiang et al., 2023). Table 3 shows the common mode voltage with respect to the virtual mid–point potential of the rectified dc voltage ($v_{no}$) for different switching states. The mid–point terminal has been marked as "o" in the Fig. 1. As evident from the Table 3, the voltage ($v_{no}$) depends on the boost-factor "B". Another important point is that the voltage ($v_{no}$) in the different zero states and shoot–through states do not cancel in a switching cycle due to constant negative voltage during the shoot–through states. The CMV is the summation of the common mode voltage ($v_{no}$) due to inverter switching and the common mode voltage ($v_{og}$) due to bridge rectifier (Akagi et al., 2004). The boosted dc bus voltage ($v_{dcbus}$) is shown in the Fig. 8(a). The waveform of the voltage ($v_{no}$) is shown in the Fig. 8(b). The waveform of the voltage ($v_{og}$) is shown in Fig. 8(c). This waveform indicates the presence of low frequency component at the third harmonic of grid frequency. The CMV($v_{ng}$) waveform, as summation of the voltages in 8(b) and in Fig. 8(c), is shown in Fig. 8(d).

For a small unbalance in the grid supply, the rectified output voltage at the P–terminal with respect to the grid neutral contains a grid frequency component. This gives rise to a grid frequency component in the common mode voltage in case of grid supply unbalance. In the simulation study, root-mean-square (rms) magnitude of one of the phase voltages is increased by 5 % from its nominal value to study the effect. The instantaneous waveform of P–terminal of the rectifier ($v_{Pg}$) shows the periodic variation of the waveform with the grid frequency along with the variation at thrice of the grid frequency in the Fig. 9(a). The instantaneous voltage waveform of the virtual mid-point of the rectifier with respect to the grid neutral ($v_{og}$) shows the periodic variation of the waveform with the grid frequency component along with the variation of the frequency component at thrice of the grid frequency in Fig. 9(b).

The presence of the frequency component at third harmonic of the grid frequency is inevitable even if the dc voltage is created using SVPWM rectifier, as the three phase voltages at the ac end of the rectifier contains the frequency component at third harmonic of the grid frequency (Acharya et al., 2010; Hedayati et al., 2013).

The low frequency harmonic spectrum of the output line–to–line voltage obtained from simulation is shown in Fig. 10. The rms magnitude of the desired frequency of 80 Hz is nearly equal to 90 V.

The low frequency harmonic spectrum of the CMV is shown in Fig. 11. The dominant low frequency components are of frequencies at third harmonic of grid frequency and at third harmonic of the desired frequency.

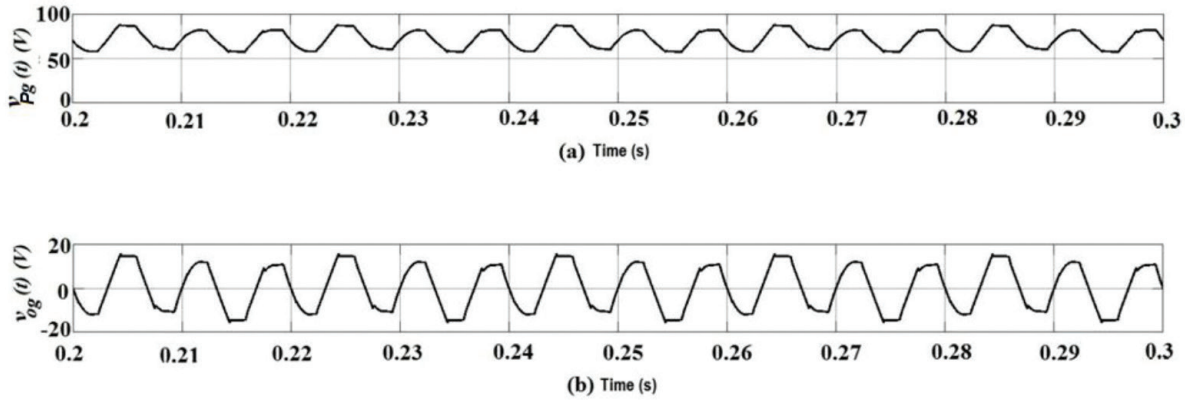


**Fig. 9.** (a) The waveform of the voltage at the P-terminal of the rectifier with respect to the ac grid neutral ($v_{pg}$), (b) The waveform of the virtual mid-point potential of the rectified voltage with respect to the ac grid neutral ($v_{og}$). Grid voltage: Phase–U 61 *V*, Phase–*V* 58 V, Phase–*W* 58 V, 50 Hz, Shoot-through duty ratio: 0.1, modulation index: 0.8 and desired output voltage frequency: 80 Hz.

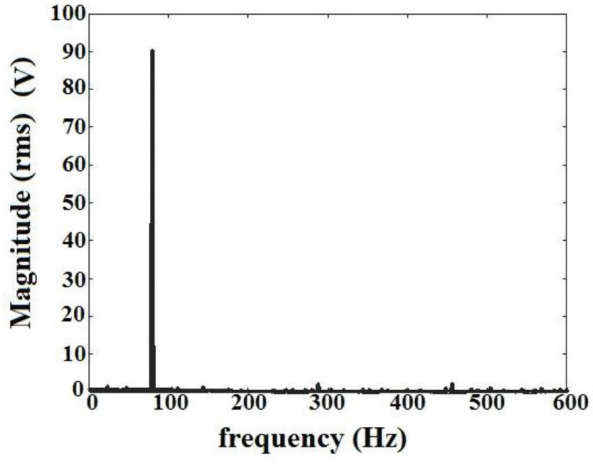


**Fig. 10.** Simulation result: Low frequency harmonic spectrum of the output line–to–line voltage. Shoot-through duty ratio 0.1. Output frequency 80 Hz. Modulation index m = 0.8. Three-phase ac voltage at the input of the diode bridge rectifier: 100 V (line–to–line), 50 Hz.

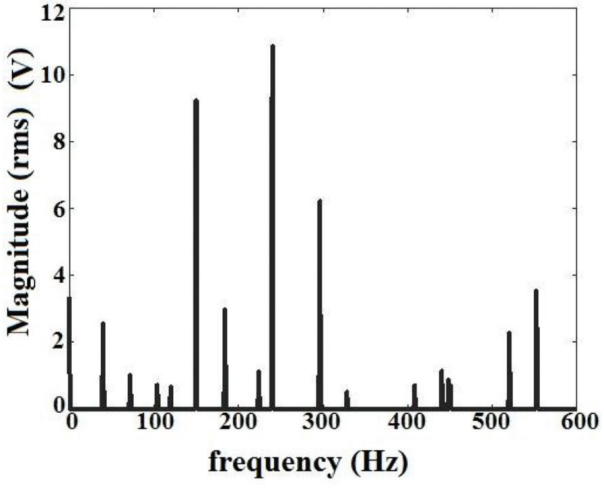


**Fig. 11.** Simulation result: Low frequency harmonic spectrum of the common mode voltage ($v_{ng}$). Shoot-through duty ratio 0.1. Output desired frequency 80 Hz. Modulation index m = 0.8. Three-phase ac voltage at the input of the diode bridge rectifier: 100 V (line–to–line), 50 Hz.

**Table 4.** Simulation Results.

| Output Frequency | Rectified dc voltage | Shoot-through duty ratio | Boosted dc voltage | Output voltage (L-L) Magnitude (rms) | Dominant Low frequency Components in the CMV | |
|---|---|---|---|---|---|---|
| | | | | | Frequency | Magnitude (rms) |
| 40 Hz | 138 V | 0.05 | 144 V | 81 V | 120 Hz<br>150 Hz | 8 V<br>10 V |
| | 138 V | 0.1 | 160 V | 90 V | 120 Hz<br>150 Hz | 9 V<br>10 V |
| | 138 V | 0.15 | 178 V | 100 V | 120 Hz<br>150 Hz | 10 V<br>10 V |
| 50 Hz | 138 V | 0.05 | 144 V | 81 V | 150 Hz<br>150 Hz | 13 V<br>13 V |
| | 138 V | 0.1 | 160 V | 90 V | 150 Hz<br>150 Hz | 14 V<br>14 V |
| | 138 V | 0.15 | 178 V | 100 V | 150 Hz<br>150 Hz | 15 V<br>15 V |
| 80 Hz | 138 V | 0.05 | 144 V | 81 V | 240 Hz<br>150 Hz | 10 V<br>10 V |
| | 138 V | 0.1 | 160 V | 90 V | 240 Hz<br>150 Hz | 10 V<br>9 V |
| | 138 V | 0.15 | 180 V | 102 V | 240 Hz<br>150 Hz | 11 V<br>9 V |

The several simulations are run at different output frequencies of 40 Hz, 50 Hz and 80 Hz and at different shoot–through duty ratios of 0.05, 0.1 and 0.15. The modulation index is maintained at 0.8 for all the cases. The results are tabulated in the Table 4. The values are rounded off to the nearest integer. The values of the rectified dc voltage, the boosted dc voltage, the rms magnitude of the output line–to–line voltages and the rms magnitudes of the different dominant low frequency components in the CMV are tabulated. In all the cases, the 100V, 50 Hz three phase voltages are applied at the input of the diode bridge rectifier.

The theoretical rectified dc average value without any filter and ideal diodes is 135 V for a bridge rectifier with 100 V, 50 Hz three phase voltages. The value obtained in simulation is nearly equal to the theoretical value.

The boosted dc voltages are nearly equal to the theoretical values. For example, considering 80 Hz output frequency and 0.1 shoot through duty ratio, from (2) and (3), the boosted dc voltage should be around 172 V. The value obtained from simulation study is 160 V. The small drop in the value can be attributed to the voltage drop in the resistance of the inductor and voltage drop across the diode in the Z-network.

Theoretically, for ideal switches, the rms magnitude of the output line-to-line voltage with boosted dc voltage of 160 V and 0.8 modulation index is a 90.52 V. The voltage obtained through simulation is around 90 V.

# 4. Experimental results

Experiments were carried out in the laboratory with a Q–ZSI stack built in the laboratory consisting of a three phase diode bridge rectifier feeding a Q–ZSI. A photograph of the experimental setup is shown in Fig. 12. The power circuit schematic of the Q–ZSI stack is closely similar to Fig. 1. Only two diodes in series are used in the experimental setup instead of one diode marked as “D7” in the power schematic.

LEM voltage sensors are used to sense different voltages for capturing waveforms in a digital storage oscilloscope. The gain of each voltage sensor employed is 7.125 mV/V. The instantaneous voltage waveforms from the output of the voltage sensors are captured in a digital storage oscilloscope. A Norma D6200 Power Analyser computes the harmonic spectrum of the common mode voltage. The ratings of the circuit components and semiconductor devices considered for experimental study are given in Table 5.

The rectified dc voltage waveform at the input of the Q-ZSI and the boosted dc voltage waveform obtained experimentally are shown in Fig. 13. The ac line-to-line voltage is maintained at 100V (L–L), 50 Hz and shoot-through duty ratio is set at 0.1by programming through a real–time field programmable gates array (FPGA) based controller. The SVPWM switching frequency real–time controlled at 5 kHz. As recorded in Trace-1, the output of

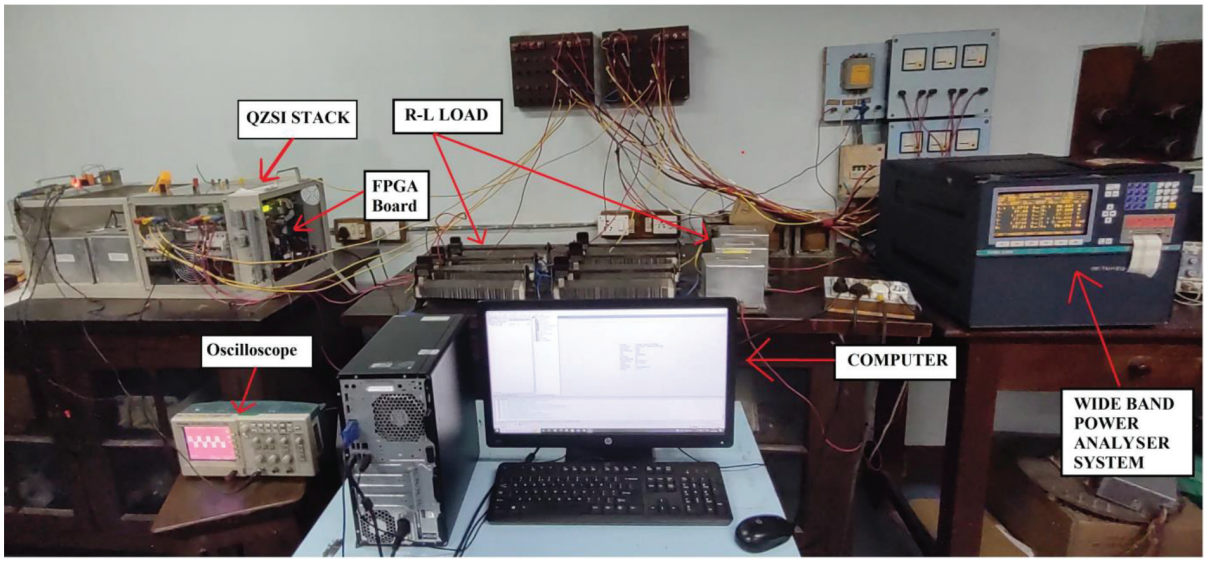


**Fig. 12.** Experimental setup.

**Table 5.** Rating of the electrical circuit components and semiconductor devices.

| Circuit components and semiconductor devices | Rating |
|---|---|
| dc filter capacitor ($C_{in}$) | 2000 microF, 450 V |
| Z–network inductor ($L_1$) | 20 mH, 20 A dc |
| Z–network inductor ($L_2$) | 20 mH, 20 A dc |
| Capacitance of Z–network capacitor ($C_1$) | 140 microF, 1800 Vdc |
| Capacitance of Z–network capacitor ($C_2$) | 140 microF, 1800 V dc |
| Inductor of the per phase load ($Z_L$) | 20 mH, 5 A |
| Resistor of the per phase load ($Z_L$) | 29 ohms, 6 A |
| Bridge rectifier diode | 80 A, 1600 V |
| Z-network diode | 150 A, 1200 V |
| IGBT in the H-bridge inverter | 100 A, 1200 V |

the voltage sensor for rectified dc voltage is 0.95V. Considering the gain of the voltage sensor as 7.125 mV/V, the rectified voltage is 133 V, which is close to the theoretical value of 135 V for a three-phase bridge rectifier. As recorded in Trace–2, the output of the voltage sensor for the boosted dc voltage during non-shoot-through time interval is 1.16V. Considering the gain of the LEM voltage sensor as 7.125 mV/V, the boosted dc voltage is 162.8 V. Theoretically, the boosted dc voltage should be166.25 V with a shoot-through duty ratio 0.1 and rectifier output of 133 V. But due to the dc voltage drop in the equivalent series resistance of the inductors and across the diode of Z-network, the ideal boosting is not obtained.

The line–to–line output voltage waveform and the waveform for the voltage across the per–phase load, as sensed by the voltage sensors, are shown in Fig. 14.

The CMV voltage waveform along with the output line–to–line voltage wave form as sensed by the voltage sensors, are shown in Fig. 15. The envelope of the CMV waveform clearly indicates the presence of third harmonic at the grid frequency.

The low frequency harmonic spectrum of the output line–to–line voltage is shown in Fig. 16. The rms magnitude of the desired frequency of 80 Hz is nearly equal to 77 V.

The low frequency harmonic spectrum of the CMV is shown in Fig. 17. The dominant low frequency components are of frequencies at third harmonic of grid frequency and at third harmonic of the desired frequency.

The several experiments are carried out for different output frequencies of 40 Hz, 50 Hz and 80 Hz and different shoot–through duty ratios of 0.05, 0.1 and 0.15. The modulation index is maintained at 0.8 for all the cases.

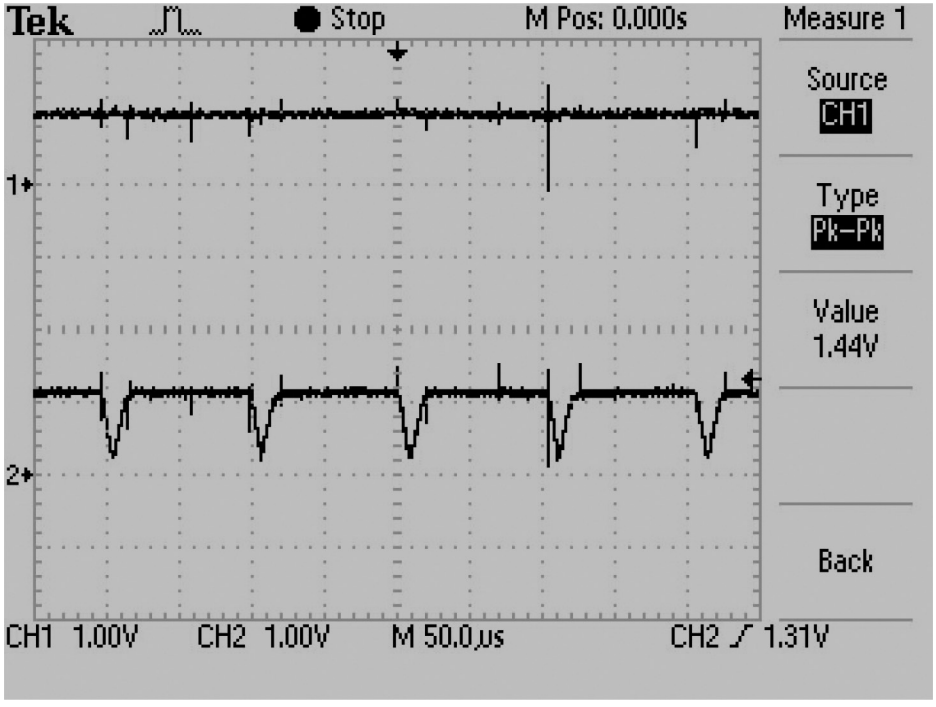


**Fig. 13.** Experimental waveforms: Trace–1: Voltage sensor output for the rectified dc voltage, Trace–2: Voltage sensor output for boosted dc voltage with shoot-through duty ratio 0.1. Voltage sensor gain: 7.125 mV/V.Three–phase ac voltage at the input of the diode bridge rectifier: 100 V (line–to–line), 50Hz.

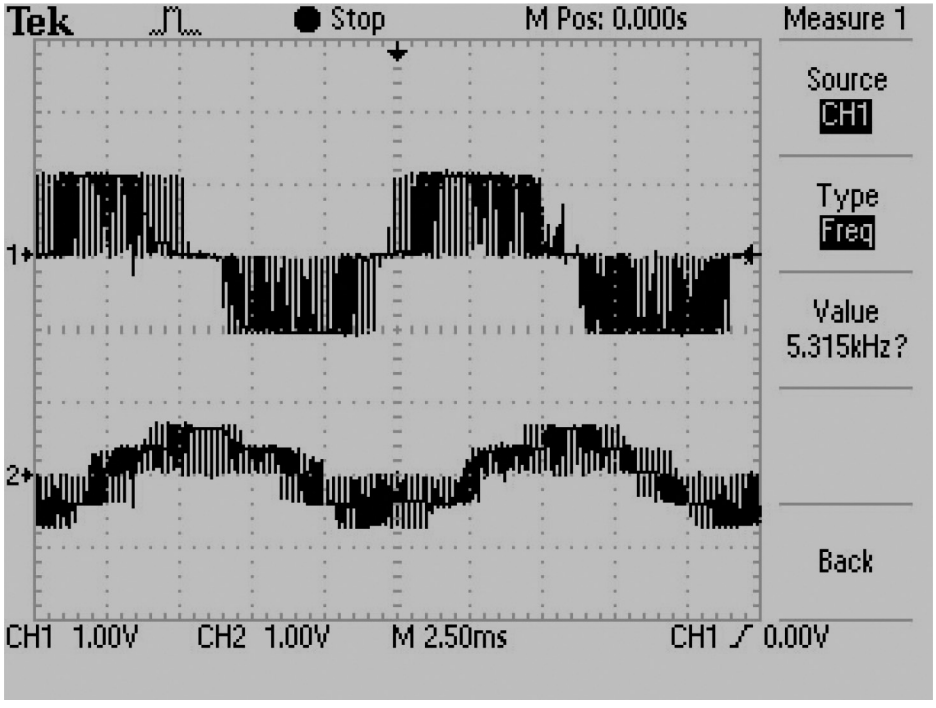


**Fig. 14.** Experimental waveforms: Trace–1: Voltage sensor output for the output line–to–line voltage.Trace–2: Voltage sensor output for the voltage across the per-phase load. Voltage sensor gain: 7.125 mV/V. Shoot-through duty ratio 0.1. Output desired frequency 80 Hz. Modulation index m = 0.8. Three-phase ac voltage at the input of the diode bridge rectifier: 100 V (line–to–line), 50 Hz.

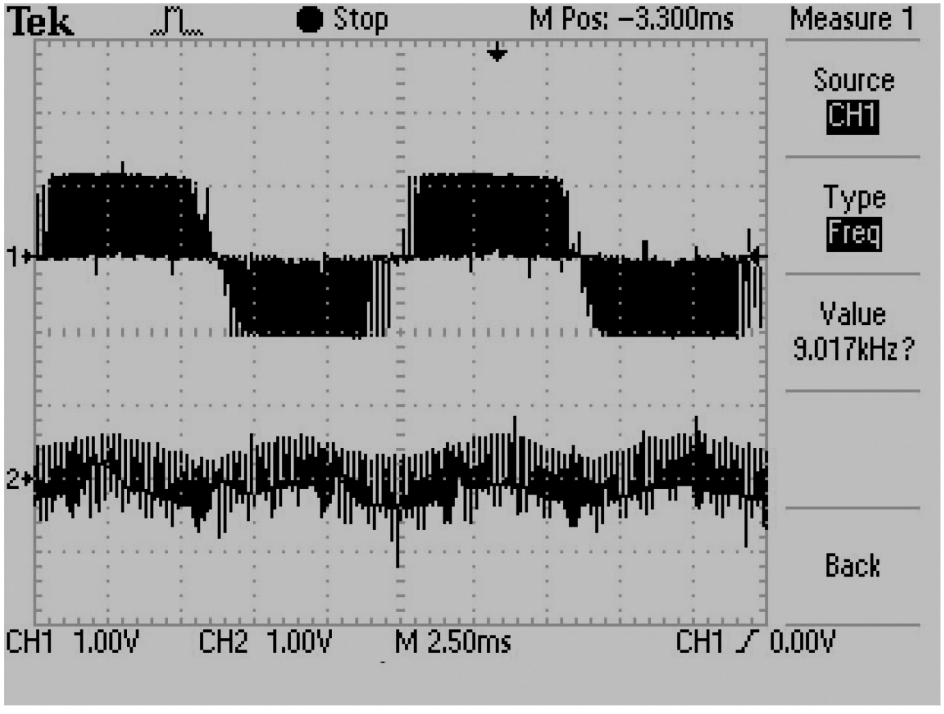


**Fig. 15.** Experimental waveforms: Trace–1: Voltage sensor output for the output line–to–line voltage, Trace–2: Voltage sensor output for CMV. Voltage sensor gain: 7.125 mV/V.Shoot-through duty ratio 0.1. Output desired frequency 80 Hz. Modulation index m = 0.8. Three-phase ac voltage at the input of the diode bridge rectifier: 100 V (line–to–line), 50 Hz.

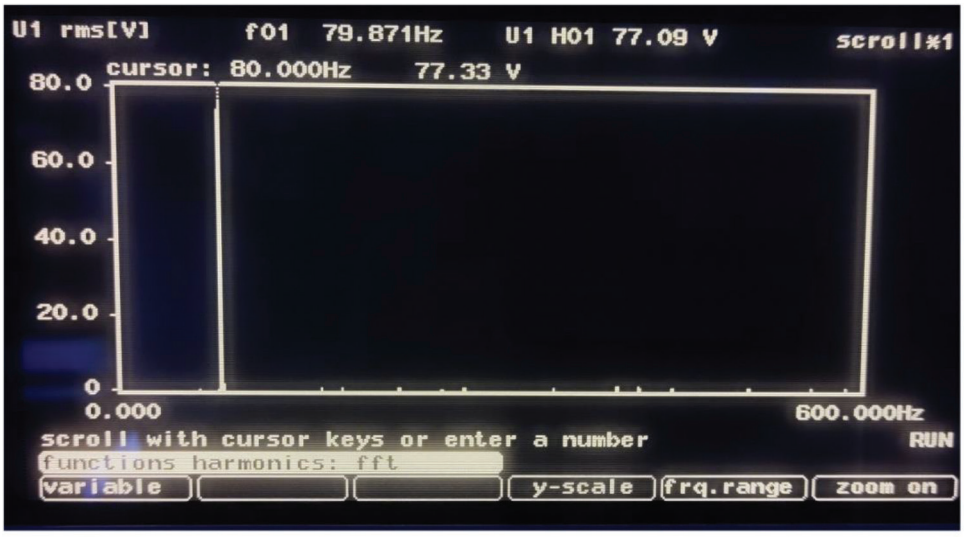


**Fig. 16.** Experimental result: Low frequency harmonic spectrum of the output line–to–line voltage analysed through Norma D6200 Power Analyser. Shoot-through duty ratio 0.1. Output desired frequency 80 Hz. Modulation index m = 0.8. Three-phase ac voltage at the input of the diode bridge rectifier: 100 V (line–to–line), 50 Hz.

The results are tabulated in the Table 6. The values are rounded off to the nearest integer. The values of the rectified dc voltage, the boosted dc voltage, the rms magnitude of the output line–to–line voltages and the rms magnitudes of the different dominant low frequency components in the CMV are tabulated. In all the cases, the 100V$\pm$ 1V, 50 Hz three phase voltages are applied at the input of the diode bridge rectifier.

The theoretical rectified dc average value without any filter and ideal diodes is 135 V for a bridge rectifier with 100 V, 50 Hz three phase voltages. The value obtained is nearly equal to the theoretical value. The small drop in

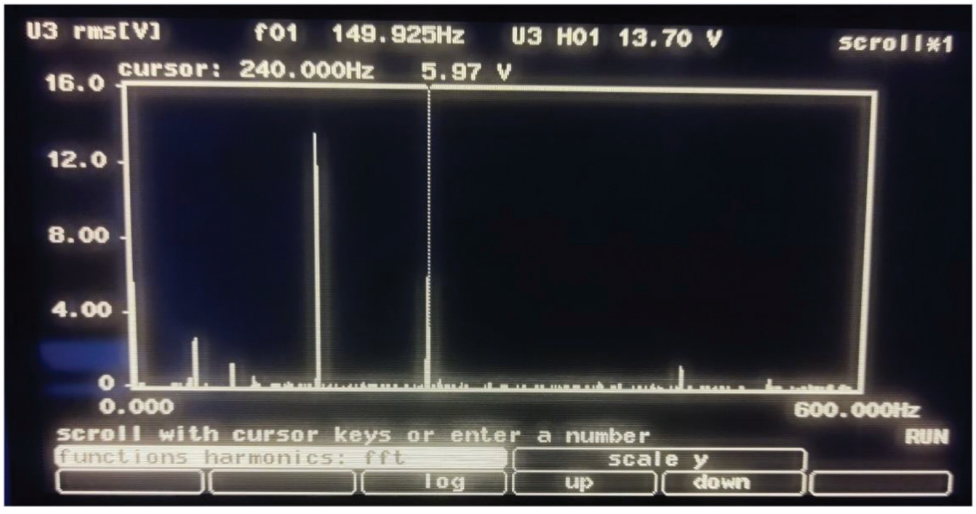


**Fig. 17.** Experimental result: Low frequency harmonic spectrum of the common mode voltage analysed through Norma D6200 Power Analyser. Shoot-through duty ratio 0.1. Output desired frequency 80 Hz. Modulation index m = 0.8. Three-phase ac voltage at the input of the diode bridge rectifier: 100 V (line–to–line), 50 Hz.

**Table 6.** Experimental Results.

| Output Frequency | Rectified dc voltage | Shoot-through duty ratio | Boosted dc voltage | Output voltage (L-L) Magnitude (rms) | Dominant Low frequency Components in the CMV | |
|---|---|---|---|---|---|---|
| | | | | | Frequency | Magnitude (rms) |
| 40 Hz | 133 V | 0.05 | 143 V | 72 V | 120 Hz<br>150 Hz | 7 V<br>14 V |
| | 133 V | 0.1 | 162 V | 78 V | 120 Hz<br>150 Hz | 8 V<br>14 V |
| | 132 V | 0.15 | 179 V | 88 V | 120 Hz<br>150 Hz | 9 V<br>15 V |
| 50 Hz | 133 V | 0.05 | 143 V | 72 V | 150 Hz<br>150 Hz | 13 V<br>13 V |
| | 133 V | 0.1 | 162 V | 79 V | 150 Hz<br>150 Hz | 13 V<br>13 V |
| | 132 V | 0.15 | 180 V | 88 V | 150 Hz<br>150 Hz | 16 V<br>16 V |
| 80 Hz | 133 V | 0.05 | 144 V | 74 V | 240 Hz<br>150 Hz | 6 V<br>13 V |
| | 133 V | 0.1 | 163 V | 78 V | 240 Hz<br>150 Hz | 6 V<br>14 V |
| | 132 V | 0.15 | 181 V | 88 V | 240 Hz<br>150 Hz | 8 V<br>14 V |

the value can be attributed to the voltage drop across the diodes and to the non-zero commutation interval due to ac source inductance (Mohan et al., 2003).

The boosted dc voltages are nearly equal to the theoretical values. For example, considering 40 Hz output frequency and 0.1 shoot through duty ratio, from (2) and (3), the boosted dc voltage should be 166.25 V. The value obtained from experiment is 162 V. The small drop in the value can be attributed to the voltage drop in the resistance of the inductor and voltage drop across the two diodes in the Z-network where “D7” is realized with two series diodes.

Theoretically, for ideal switches, the rms magnitude of the output line-to-line voltage with boosted dc voltage of 162 V and 0.8 modulation index is 91.65 V. But, the voltage obtained in the experiment is 78 V. The reduction in voltage can be attributed to the voltage drop across the IGBTs and to the loss of voltage during switching state

transitions between the IGBTs in a leg (Chatterjee et al., 2023a; Jeong et al., 1991). It is observed that with increase in duty ratio the rms magnitude increases with increase in boost factor as expected.

The corresponding rms magnitudes of the low frequency components at third harmonic of ac grid frequency are almost equal for all the desired frequencies of values 40 Hz and 80 Hz and for all the shoot-through duty ratios. This rms magnitude does not depend on the boost factor. The value is very close to the theoretical value of 11.89 V for 100V, 50 Hz three phase voltages. But for the desired output frequency of 50 Hz, the rms magnitude is different. This is due to the merging of two low frequency components of the CMV; one component due to the inverter and the other component due to the bridge rectifier. The frequencies of these two components become equal in this case.

The rms magnitudes of the low frequency components at the third harmonic of the output desired frequencies are almost equal for the desired frequencies 40 Hz and 80 Hz with respect to a particular shoot-through duty ratio. This rms magnitude does depend on the shoot-through duty ratio. For 0.1 shoot–through duty ratio and 162 V dc bus voltage, the theoretical value of the rms magnitude is 10.90 V (Tian et al., 2016). But, the voltage obtained in the experiment is 8 V. The reduction in voltage can be attributed to the voltage drop across the IGBTs and to the loss of voltage during switching state transitions between the IGBTs in a leg (Chatterjee et al., 2023a; Jeong et al., 1991). For the desired output frequency of 50 Hz, the rms magnitude is different. This is due to the merging of two low frequency components of the CMV; one component due to the inverter and the other component due to the bridge rectifier. The frequencies of these two components become equal in this case.

# 5. Conclusions

The study, presented in this paper, has analysed the various causes of low frequency components in the CMV of a Q-ZSI H-bridge converter fed from a three phase grid/utility-fed bridge rectifier. The dominant low frequency components in the CMV are found to be at third harmonic of the supply frequency and at third harmonic of the output desired frequency as found in the conventional H-bridge inverter fed from a three-phase bridge rectifier. The simulation results explain, with the help of various waveforms, the origin of those low frequency components in the CMV for a Q-ZSI H-bridge converter fed from a three phase grid/utility-fed bridge rectifier. The experimental results at different output desired frequency corroborate this fact. The experiments are carried out for different shoot-through duty ratios and for different output desired frequencies. The boost factors are different for different shoot-through duty ratios. Therefore, the magnitudes of the low frequency component at third harmonic of the output desired frequency are different for different shoot-through duty ratios. It is interesting to observe that the magnitudes of the low frequency component at third harmonic of the input ac grid frequency are not significantly different for different shoot-through duty ratios as those are dependent on the grid voltage. A peculiar situation arises when the output desired frequency becomes same as the grid frequency. The sinusoidal third harmonic component at the grid frequency and the sinusoidal third harmonic component at the desired frequency combine. The combined magnitude depends on the phase angle difference between those two same frequency components. The study can be extended further to devise a method to determine this phase difference. The switching state transition between two IGBTs in a leg also affects in reducing the expected output voltage magnitude as well as the magnitude of low frequency component in CMV at third harmonic of the output desired frequency. Any small unbalance in the magnitudes of three phase grid voltages creates supply frequency component in the CMD which needs to be considered in the low frequency spectrum of CMV as component of frequency as low as 30 Hz can create problem in EMC in naval ship and submarines. The thorough analysis of the origin of low frequency components in CMV is helpful for the research in mitigating of those components.

## References

Acharya, B. Anirudh and John, V. (2010). Common mode DC bus filter for Active Front-End converter. *Joint International Conference on Power Electronics, Drives and Energy Systems & 2010 Power India, New Delhi, India, 20–23 December 2010.*

Akagi, H. and Doumoto, T. (2004). An Approach to Eliminating High-Frequency Shaft Voltage and Ground Leakage Current From an Inverter-Driven Motor. *IEEE Transactions on Industry Applications*, 40(4), pp. 1162–1169.

Akagi, H. and Tamura, S. (2006).A Passive EMI Filter for Eliminating Both Bearing Current and Ground Leakage Current From an Inverter-Driven Motor. *IEEE Transactions on Power Electronics*,21(5), pp. 1459–1469.

Anderson, J. and Peng, F.Z. (2008). Four quasi–Z-Source inverters. In: *Proceedings of the IEEE Power Electronics Specialists Conference*. Greece, 15-19 June 2008.

Cacciato, M., Consoli, A., Scarcella, G. and Testa, A. (1999). Reduction of common mode currents in PWM inverter motor drives. *IEEE Transactions on Industry Applications*, 35(2), pp. 469–476.

Cacciato, M., Consoli, A., Scarcella, G., Scelba, G. and Testa, A. (2009). Modified space-vector-modulation technique for common mode currents reduction and full utilization of the DC bus. In: *Proceedings of2009 24th Annual IEEE Applied Power Electronics Conference and Exposition*. Washington, DC, USA, 15–19 February 2009.

Chatterjee, D., Chakraborty, C., Mukherjee, K., and Dalapati, S. (2023a). Current Zero-crossing Shift for Compensation of Dead-time Distortion in Pulse Width Modulated Voltage Source Inverter. *Power Electronics and Drives*, 8 (43), pp. 84–99.

Chatterjee, D., Chakraborty, C., and Dalapati, S. (2023b). Pulse Width Modulation Techniques in Two-level Voltage Source Inverters – State of the Art and Future Perspectives. *Power Electronics and Drives*, 8 (43), pp. 335–367.

Chen, F., Burgos, R. and Boroyevich, D. (2019). A Bidirectional High–Efficiency Transformer less Converter with Common–mode Decoupling for the Interconnection of AC and DC Grids. *IEEE Transactions on Power Electronics*, 34(2), pp.1317–1333.

Chen, F., Burgos, R., Boroyevich, D. and Zhang, X.(2016). Active Control of Low Frequency Common–Mode Voltage to Connect AC Utility and 380 V DC Grid. In: *IEEE Application on Power Electronics Conference and Exposition (APEC)*. Long Beach, CA, USA, 20–24 March 2016.

Fan, L., Liu, Z., Liang, Y., Li, H., Rao, B., Yin, S. and Jiang, D.(2023). Analysis and Utilization of Common–Mode Voltage in Inverters for Power Supply. *IEEE Transactions on Power Electronics*, 38(7), pp. 8811–8824.

Gajanayake, C. J., Luo, F. L., Gooi, H. B., So, P. L. and Siow, L. K. (2010).Extended–Boost Z–Source Inverters. *IEEE Transactions on Power Electronics*,25(10), pp. 2642–2651.

Hava, A. M. and Un, E. (2011). A High-Performance PWM Algorithm for Common–Mode Voltage Reduction in Three–Phase Voltage Source Inverters. *IEEE Transactions on Power Electronics*, 26(7), pp. 1998–2008.

Hedayati, M. H., Acharya, A. B. and John, V. (2013). Common–Mode Filter Design for PWM Rectifier–Based Motor Drives. *IEEE Transactions on Power Electronics,*28(11), pp. 5364–5371.

Hou, C-.C., Shih, C-.C., Cheng, P-.T. and Hava, A. M. (2013). Common–mode voltage reduction pulse width modulation techniques for three–phase grid connected converters. *IEEE Transactions on Power Electronics*, 28(4), pp. 1971–1979.

Huang, J. and Shi, H. (2014).Suppressing low-frequency components of common-mode voltage through reverse injection in three-phase inverter. *IET Power Electronics*, 7(6), pp. 1644–1653. 2014

Jiang, Y., Zhang, J., Wang, Q., He, F. and Zhang, W. (2023). A Common-Mode Voltage Reduction PWM Strategy for Three–Phase Quasi–Z–Source Inverter With Optimized Switching Losses. *IEEE Access.*11, pp. 91891–91903.

Jeong, Seung-Gi and Park, Min-Ho. (1991). The analysis and compensation of dead–time effects in PWM inverters. *IEEE Transactions on Industrial Electronics*, 38(2), pp. 108–114

Lai, Y. S. and Shyu, F. S. (2004). Optimal common–mode voltage reduction PWM technique for inverter control with consideration of the dead–time effects part I: Basic development. *IEEE Transactions on Industry Applications*, 40(6), pp. 1605–1612.

Liu, Y., Ge, B., Abu-Rub, H. and Peng, F. Z. (2014). Overview of Space Vector Modulations for Three-Phase Z-Source/Quasi-Z-Source Inverters. *IEEE Transactions on Power Electronics*, 29(4), pp. 2098–2108.

Loh, P. C., Vilathgamuwa, D. M., Lai, Y. S., Chua, G. T. and Li, Y. (2005). Pulse–Width Modulation of Z–Source Inverters. *IEEE Transactions on Power Electronics*, 20(6), pp. 1346–1355.

MIL-STD-461F, (2007). Requirements for the control of electromagnetic interference characteristics of subsystems and equipment, *Department of defense interface standard*, United States of America

Mirzaeva, G., Carter, D., Uddin, S. M. M. and Stepien, P. (2020). Common Mode Voltage Elimination in Variable Speed Drives for Improved Electrical Safety. *IEEE Transactions on Industry Applications*, 56(4), pp. 4365–4374.

Mohan, N., Underland, T. M. and Robbins, W. P. (2003). *Power Electronics Converters, Applications and Design*. John Wiley & Sons, pp 103–108.

Nanda, D., Syam, P. and Mukherjee, K. (2019). Selection procedure of Z–network parameters for a SVPWM Voltage fed ZSI under varying input voltage conditions with simulated performance. In: *Proceedings of 2019 IEEE Region 10 Symposium (TENSYMP)*.Kolkata, India, 7–9 June 2019.

Nguyen, M.-K., Lim, Y.-C. and Cho, G.-B.(2011). Switched-Inductor Quasi-Z-Source Inverter. *IEEE Transactions on Power Electronics*, 26(11), pp. 3183–3190.

Oliveira, T. R., Seleme, S. I. and Donoso-Garcia, P. F. (2017). Feed–forward active attenuation of low frequency common–mode voltages in DC micro grids. In*: Proceedings of 2017 Brazilian Power Electronics Conference (COBEP)*. Juiz de Fora, Brazil, 19–22 November 2017.

Peng, F. Z. (2003). Z-Source Inverter. *IEEE Transactions on Industry Application*. 39(2), pp. 504–510.

Peng, F. Z., Joseph, A., Wang, J., Shen, M., Chen, L., Pan, Z., Ortiz-Rivera, E. and Huang, Y.(2005a). Z–Source Inverter for Motor Drives. *IEEE Transactions on Power Electronics*, 20(4), pp. 857–863.

Peng, F. Z., Shen, M. and Qian, Z. (2005b). Maximum Boost Control of the Z-Source Inverter. *IEEE Transactions on Power Electronics*, 20(4), pp. 833–838.

Peng, F. Z., Yuan, X., Fang, X. and Qian, Z. (2003).Z–Source Inverter for Adjustable Speed Drives. *IEEE Power Electronics Letters*, 1(2), pp. 33–35.

Roomi, M. M. (2019). An Overview of Carrier-based Modulation Methods for Z-Source Inverter. *Power Electronics and Drives,* 4 (39), pp.15–31.

Sabat, J., Mangaraj, M., Barisal, A. K., Patra, A. K., and Chahattaray, A. K. (2022). Performance Evaluation of BB-QZSI Based DSTATCOM under Dynamic Load Condition. *Power Electronics and Drives*, 7 (42), pp. 43–55.

Smolenski, R., Kempski, A., and Bojarski, J., (2010). Statistical approach to discharge bearing currents, *The International Journal for Computation and Mathematics in Electrical and Electronic Engineering*, 29(3), pp. 647–666.

Tan, B., Gu, Z., Shen, K. and Ding, X. (2019).Third Harmonic Injection SPWM Based on Alternating Carrier Polarity to Suppress the Common Mode Voltage. *IEEE Access*. 7, pp. 9805–9816.

Tian, K., Wang, J., Wu, B., Xu, D., Cheng, Z. and Zargari, N. R. (2016). A Virtual Space Vector Modulation Technique for the Reduction of Common–Mode Voltages in Both Magnitude and Third-Order Component. *IEEE Transactions on Power Electronics*, 31(1), pp. 839–848.

Ün, E. and Hava, A.M. (2009). A near-state PWM method with reduced switching losses and reduced common–mode voltage for three-phase voltage source inverters. *IEEE Transactions on Industry Applications*, 45(2), pp. 782–793.

Vinnikov, D. and Roasto, I. (2011). Quasi–Z–Source–Based Isolated DC/DC Converters for Distributed Power Generation. *IEEE Transactions on Industrial Electronics*, 58(1), pp. 192–201.

Zhu, N., Kang, J., Xu, D., Wu, B. and Xiao, Y.(2012). An Integrated AC Choke Design for Common–Mode Current Suppression in Neutral–Connected Power Converter Systems. *IEEE Transactions on Power Electronics*, 27(3), pp. 1228–1236.